

09836784.051804

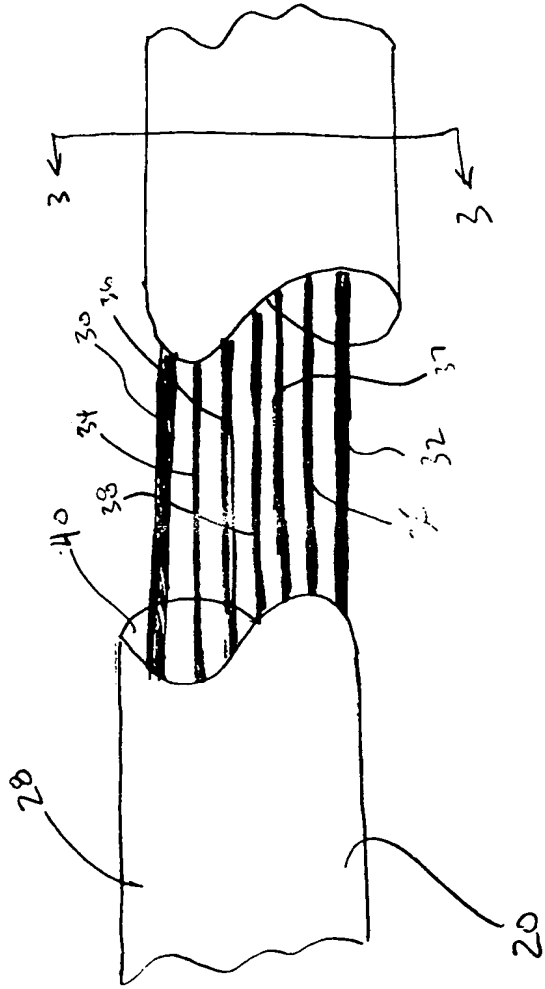


FIG. 2

09836781.061801

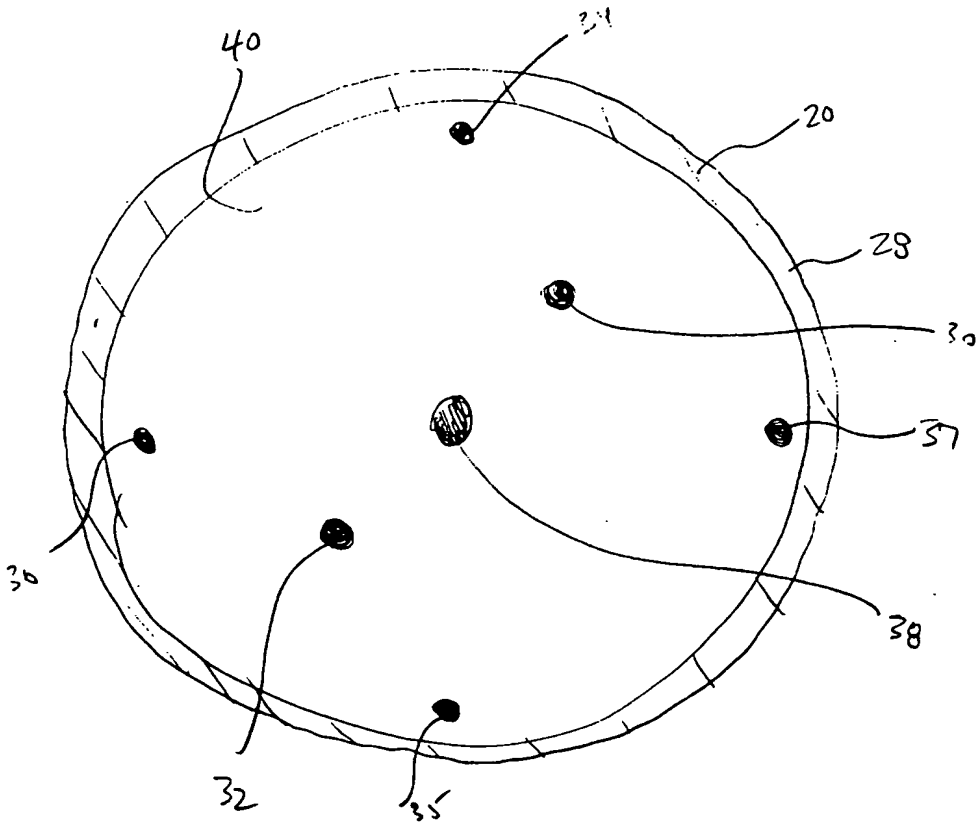


FIG. 3

09836781.061804

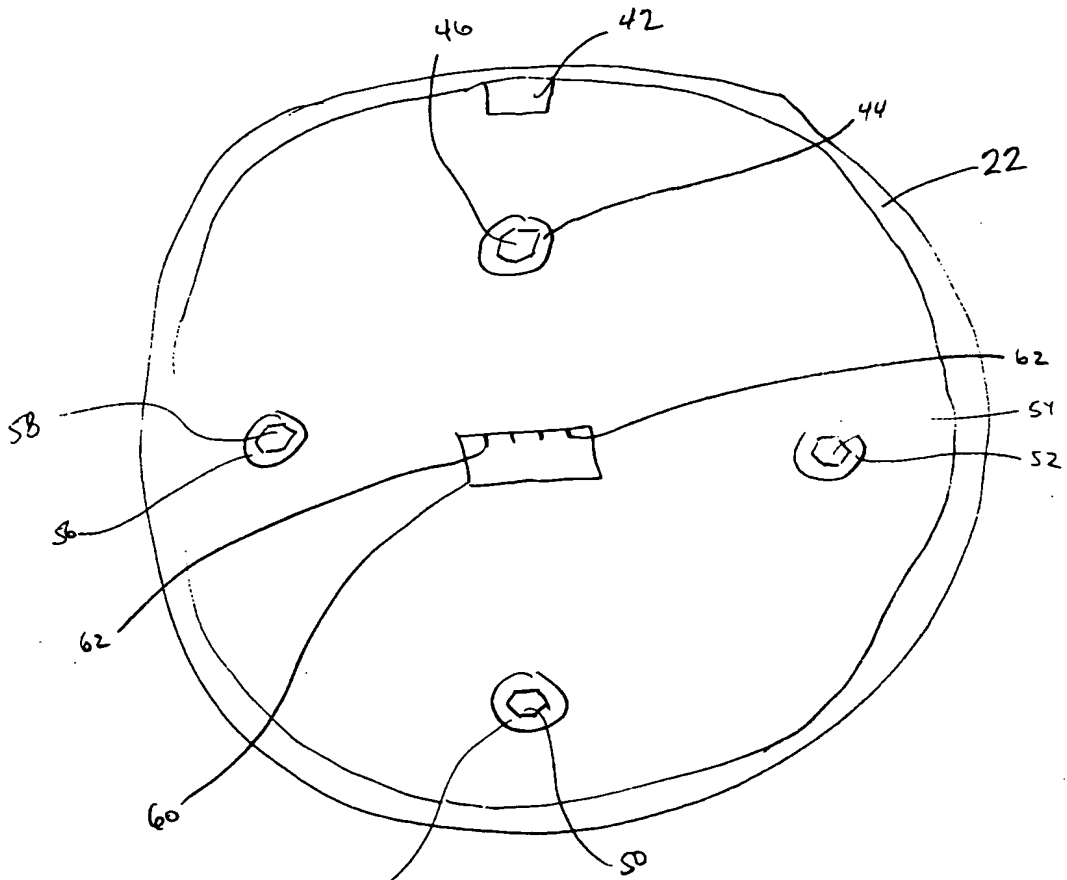


FIG. 4

098336781.054304

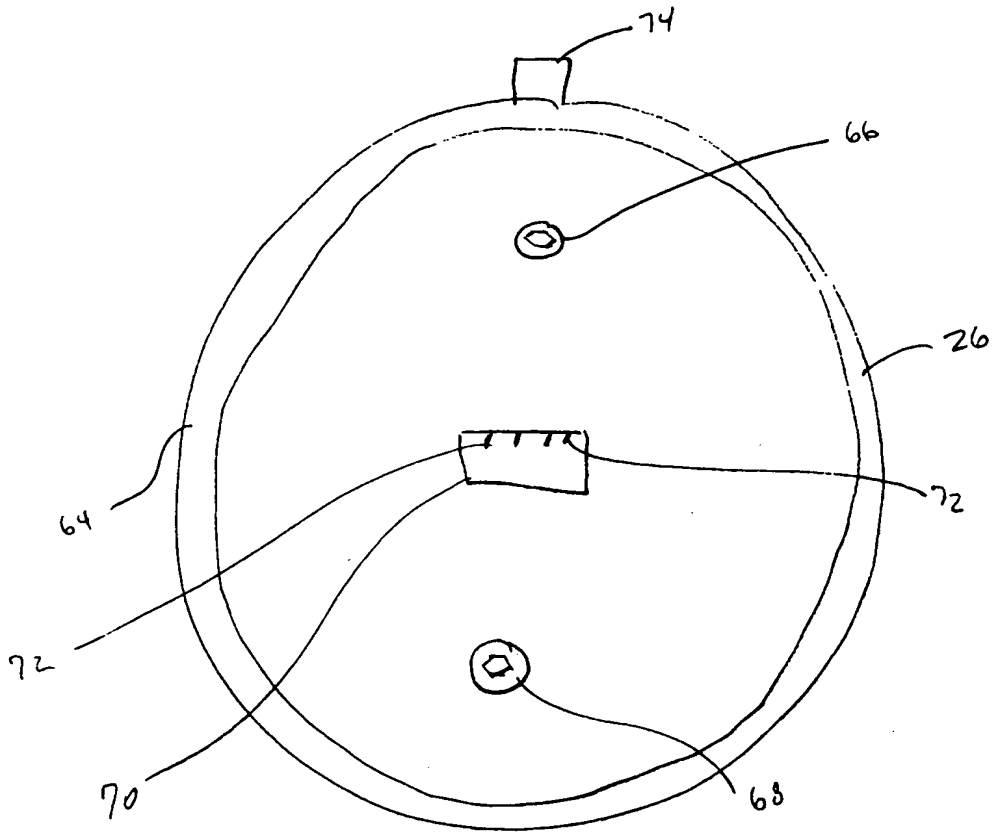


FIG. 5

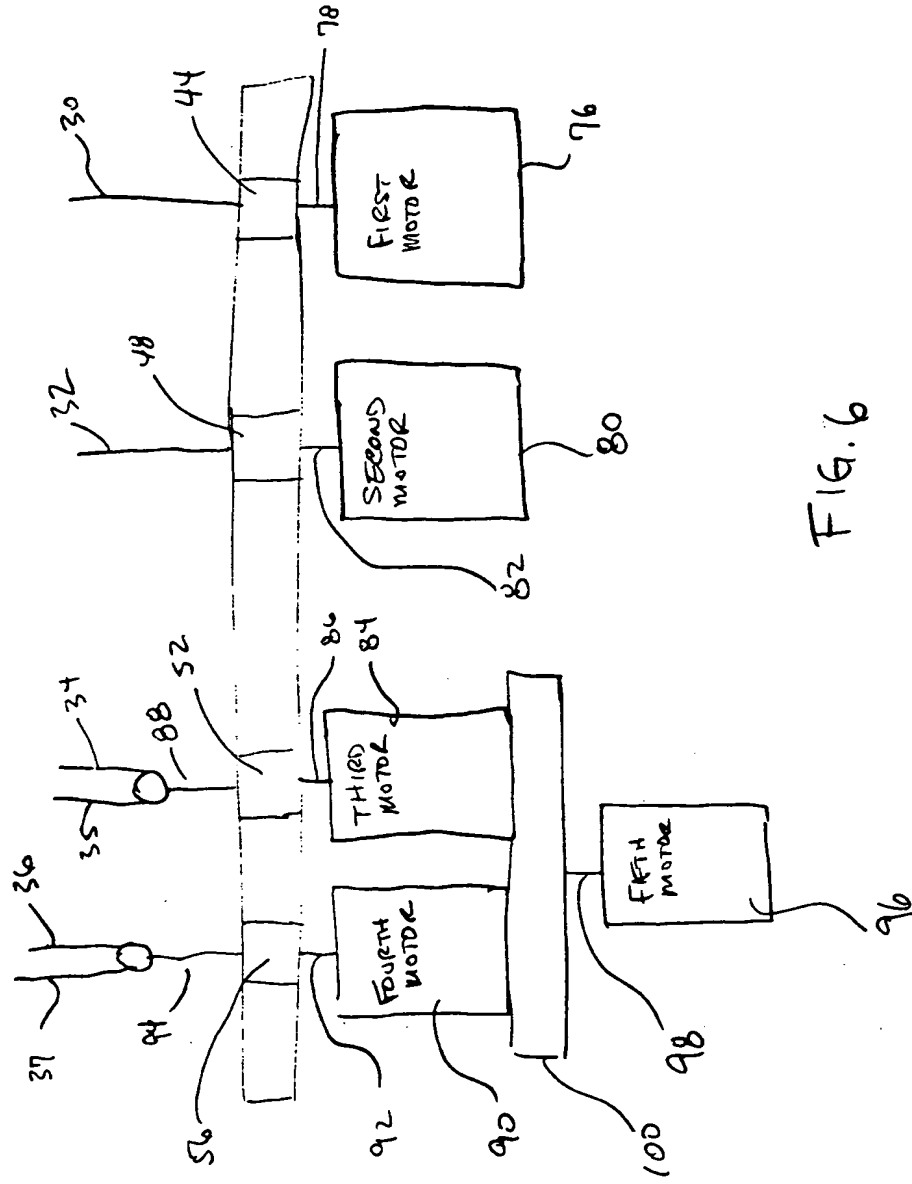


FIG. 6

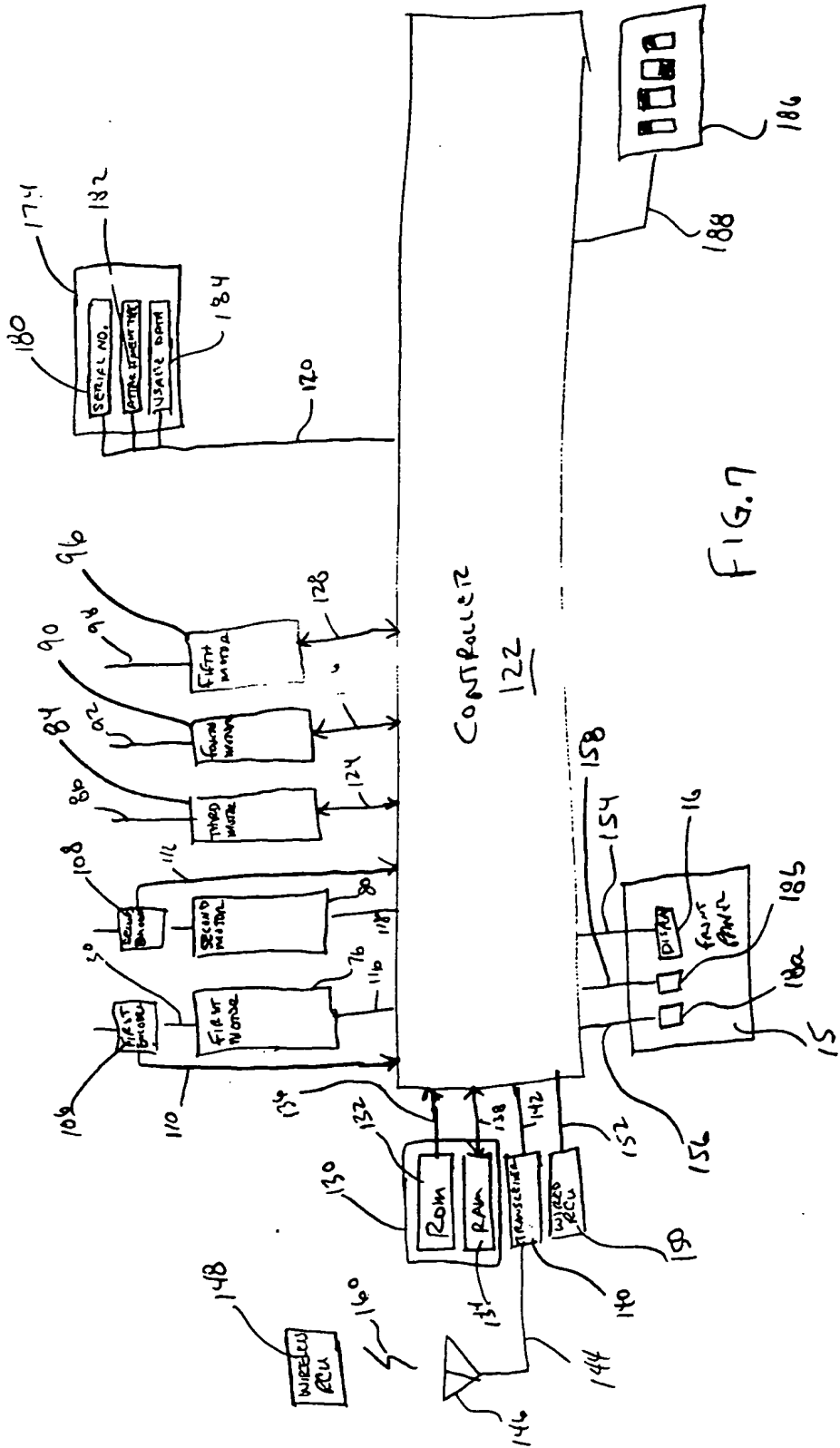


FIG. 7

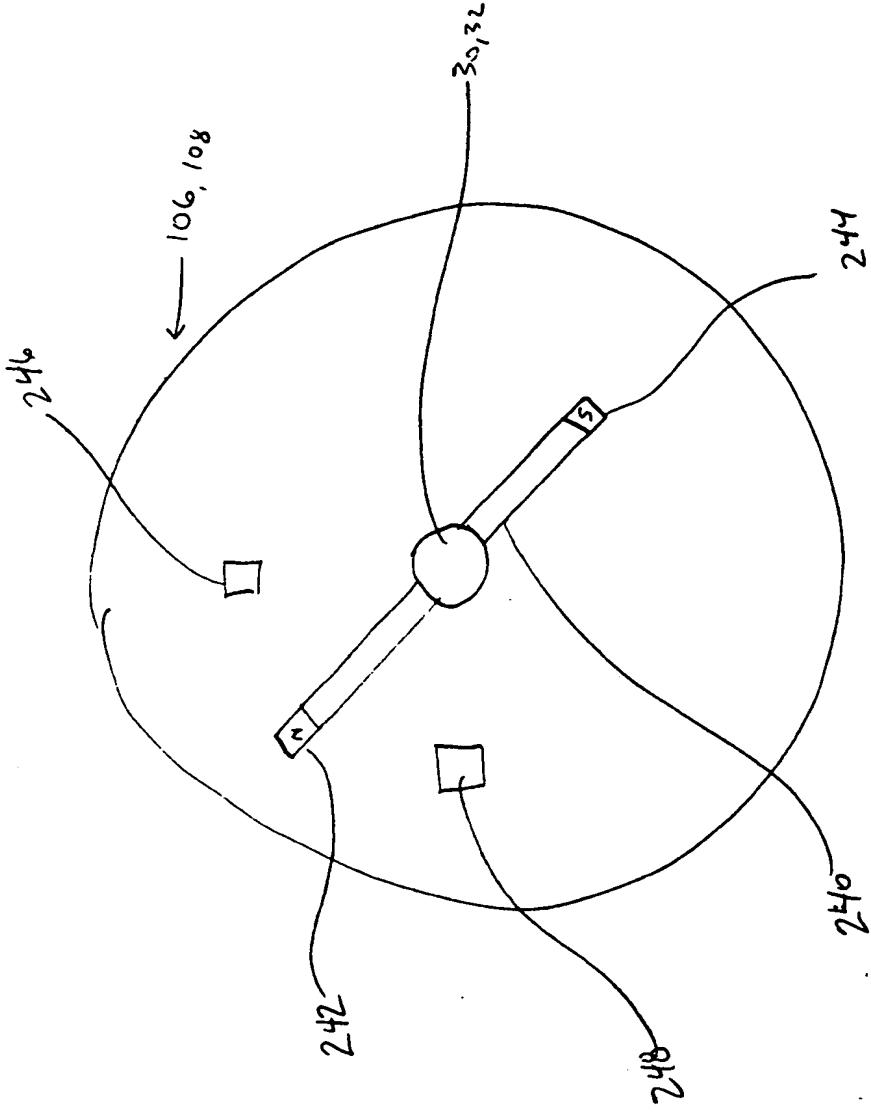


FIG. 8



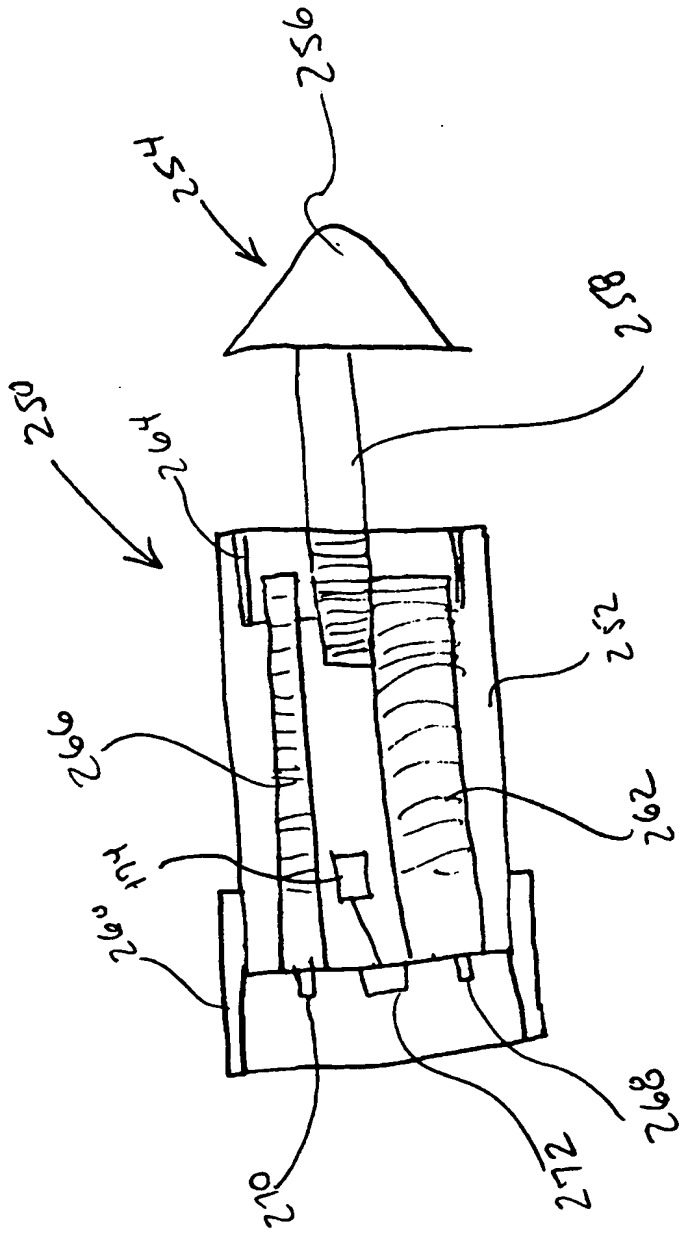


FIG. 9A



09836781, 051801

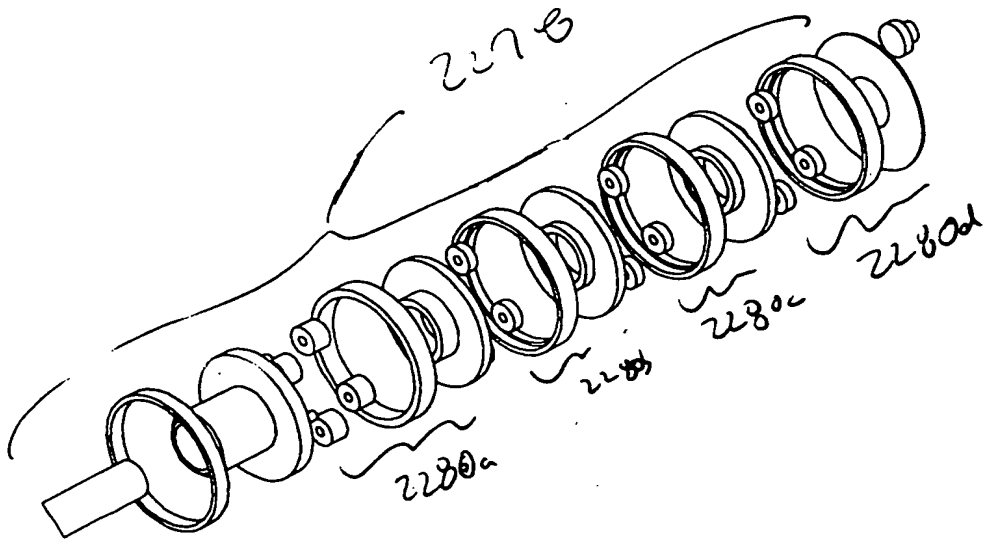


FIG. 9C

09836781, 061804

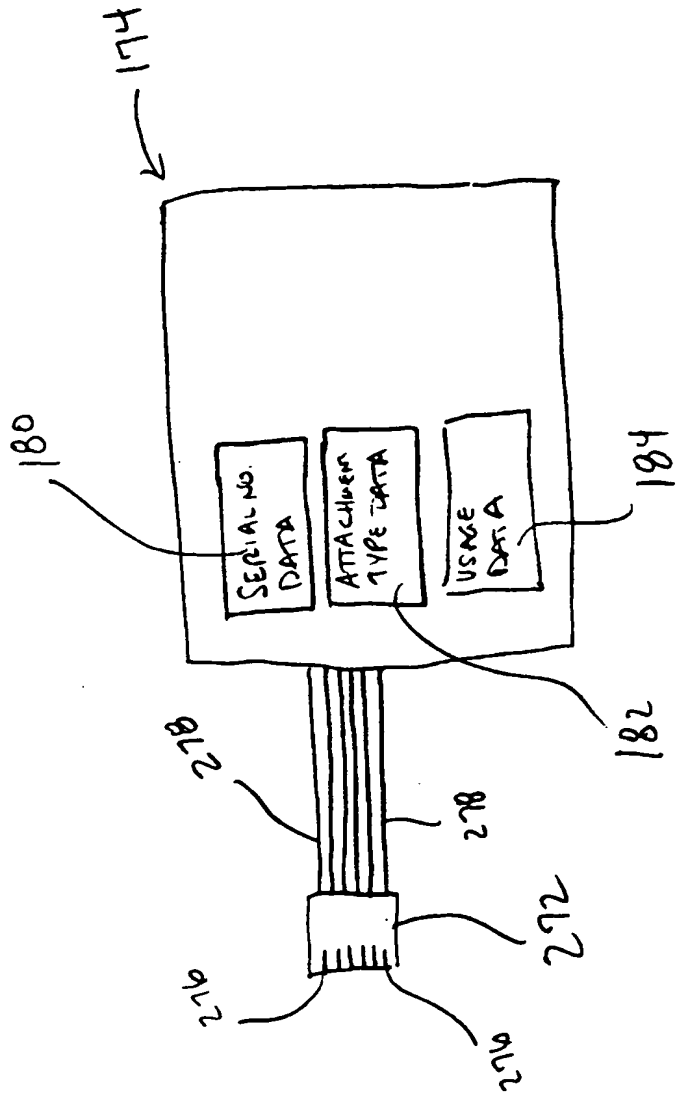


FIG. 10



09836781 061804

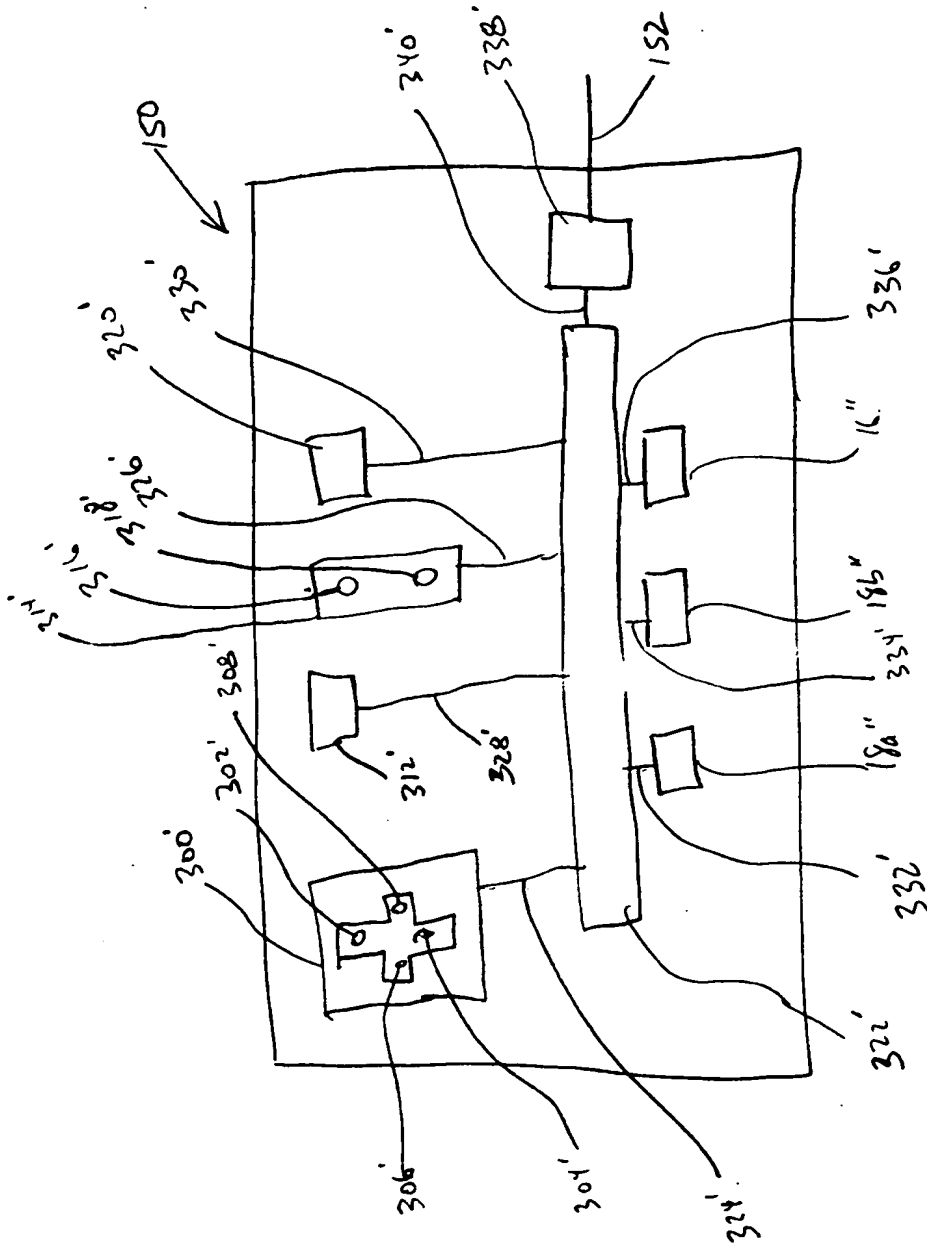


FIG. 12

09836781 061801

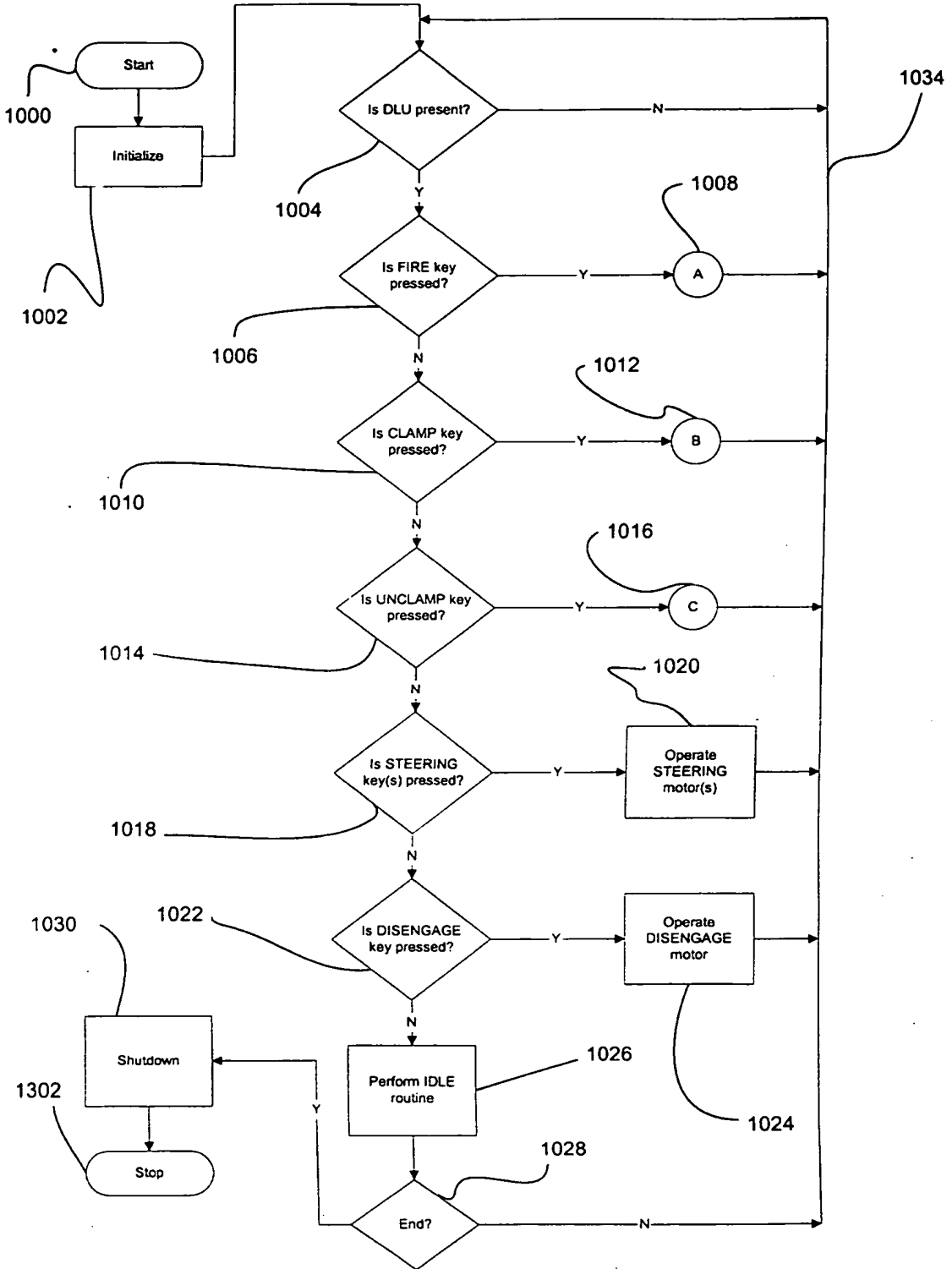


Figure 13

0936781 061301

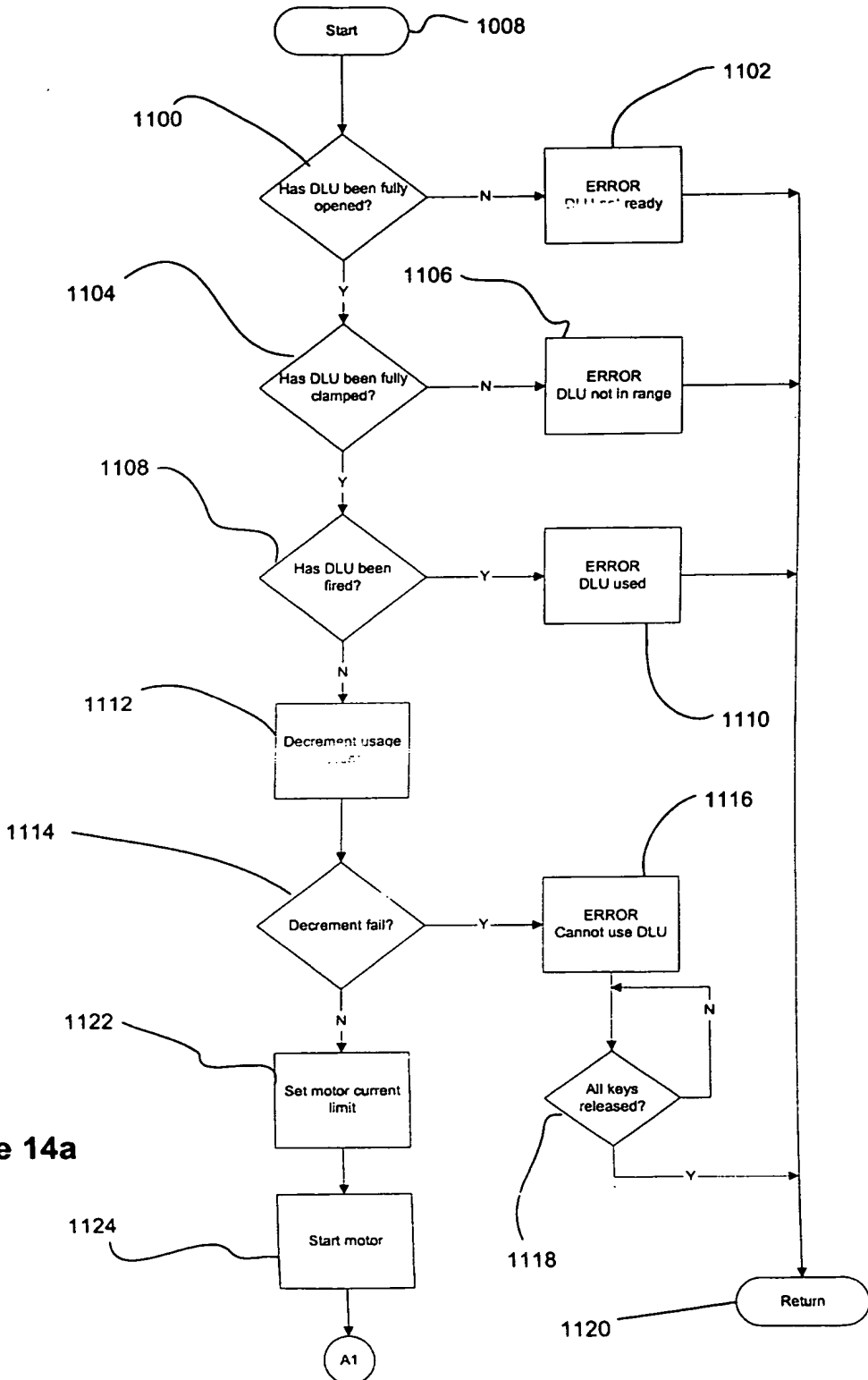


Figure 14a



09836781 061804  
108190 1879860

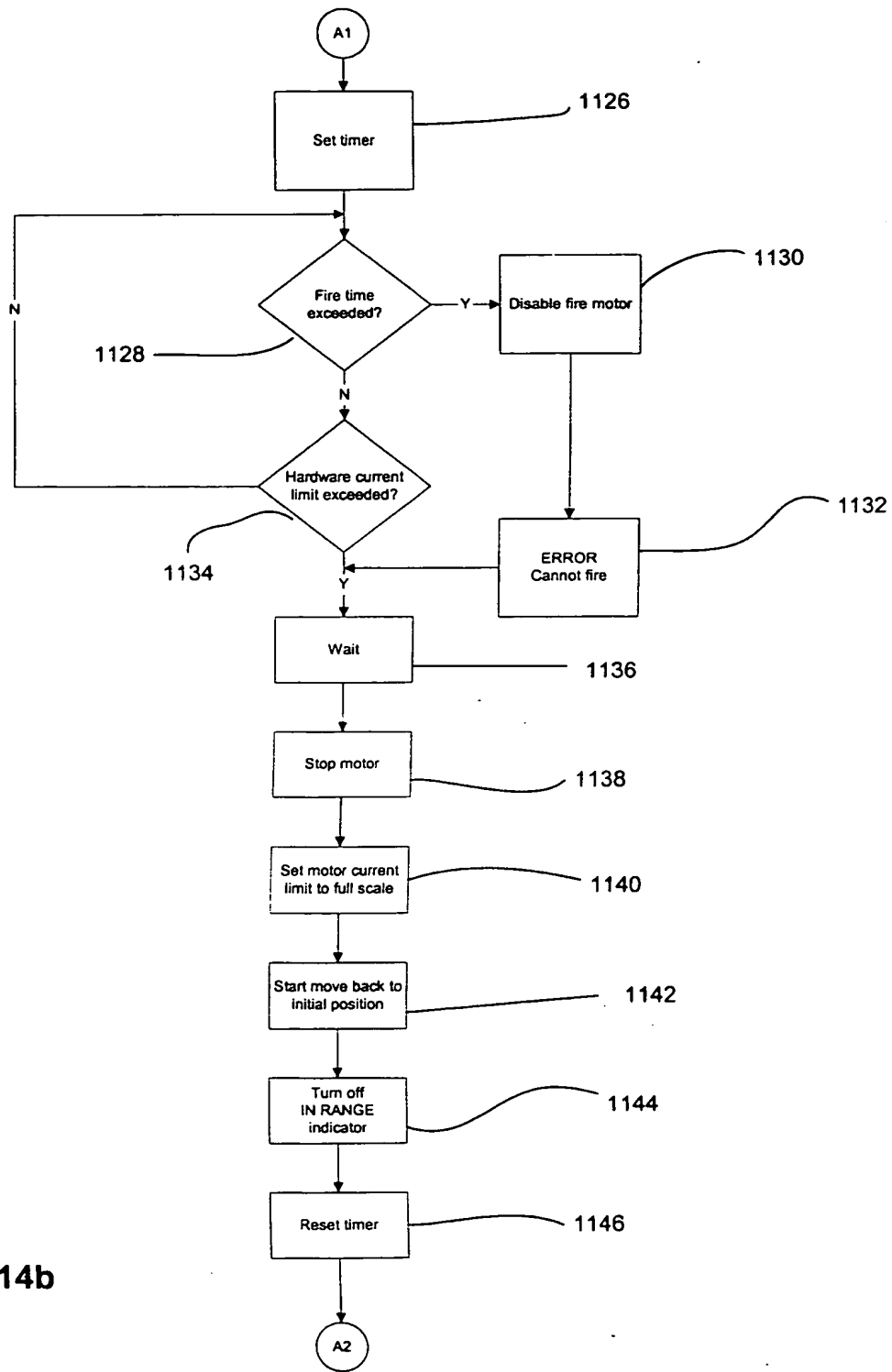


Figure 14b

09936781.054804  
FOR "90" 1879860

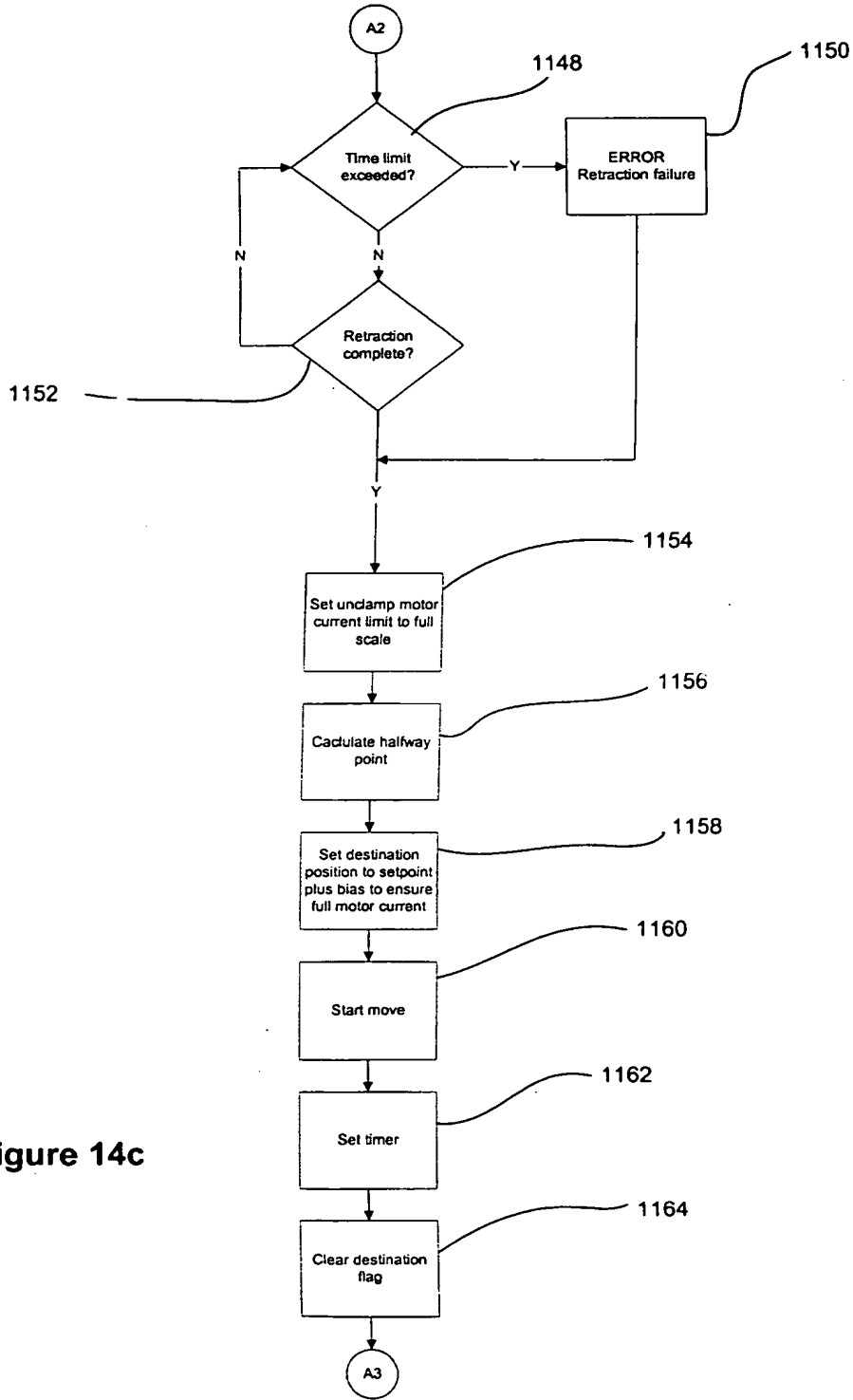


Figure 14c

09036784 061804  
FOR "T8792860

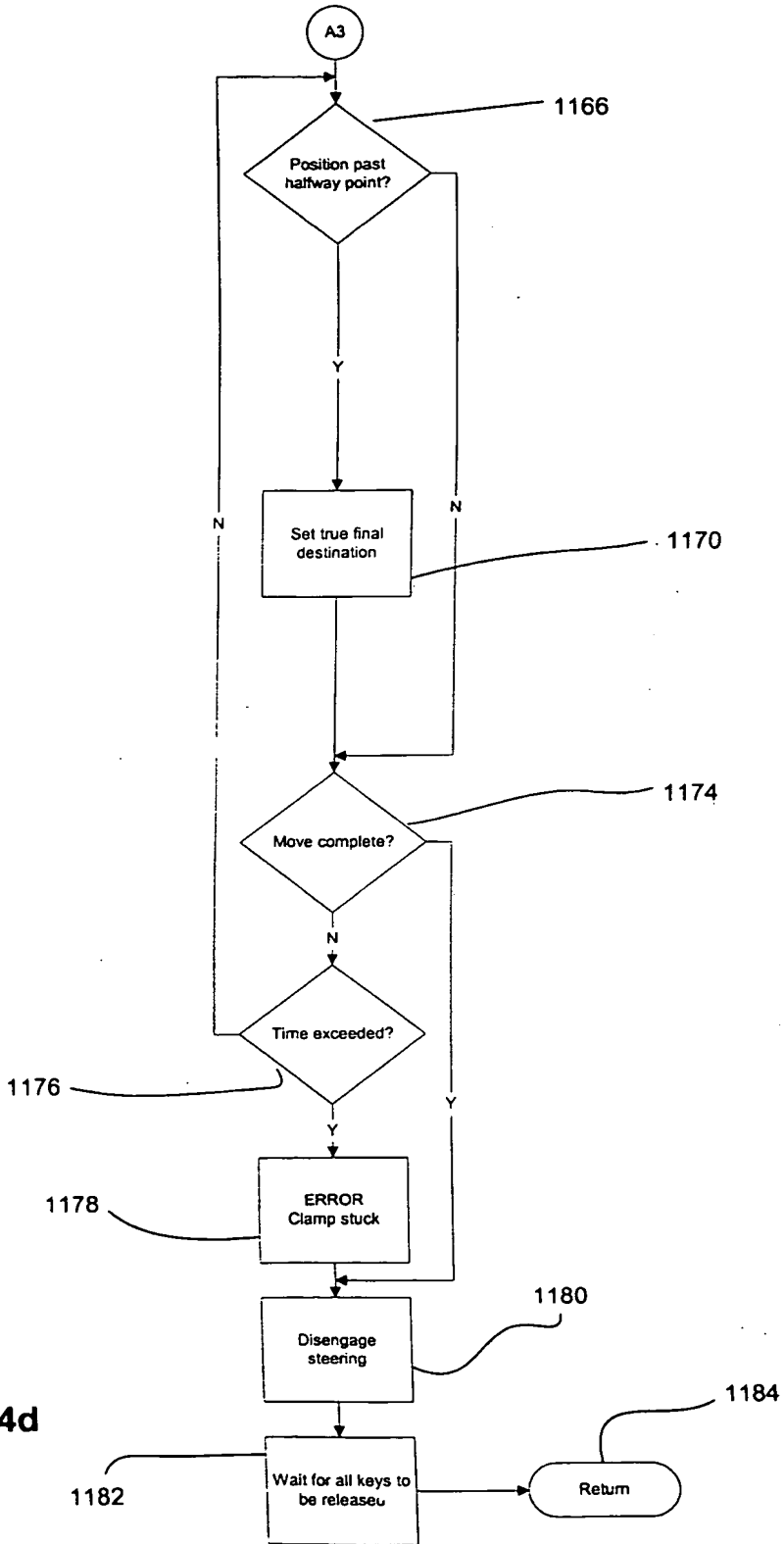


Figure 14d

09036794.061804

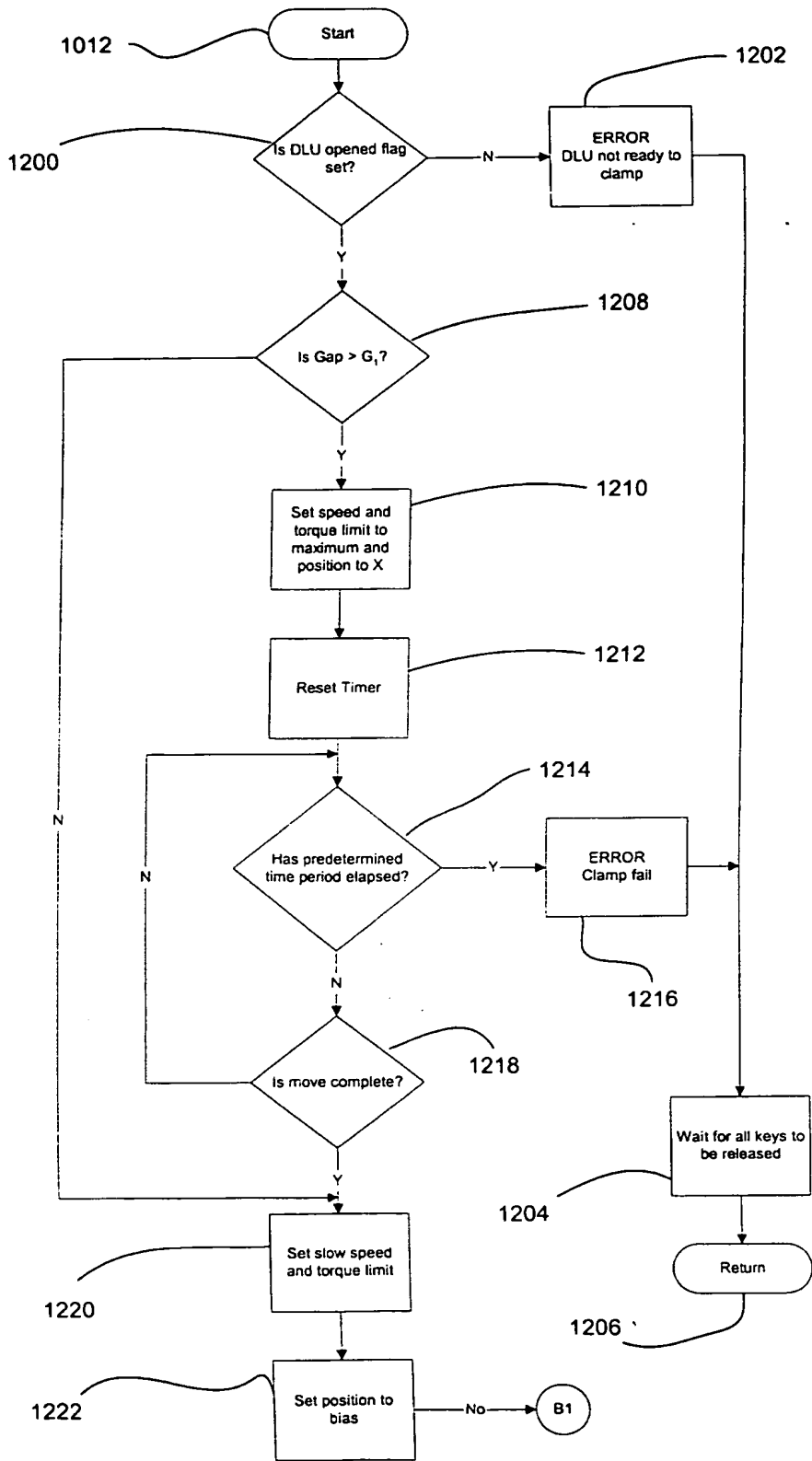


Figure 15a

09236781 061804

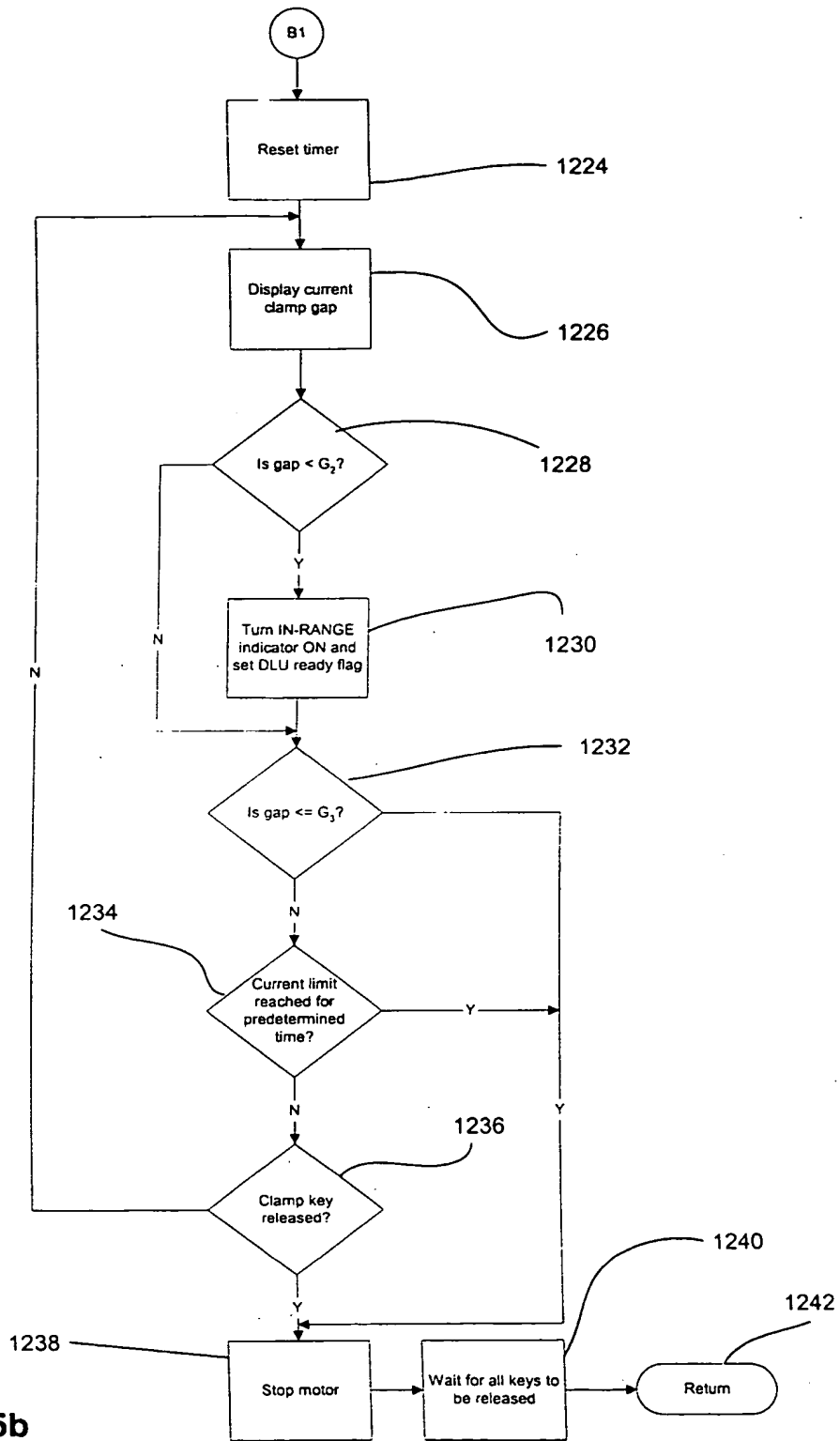


Figure 15b

09030781 061001

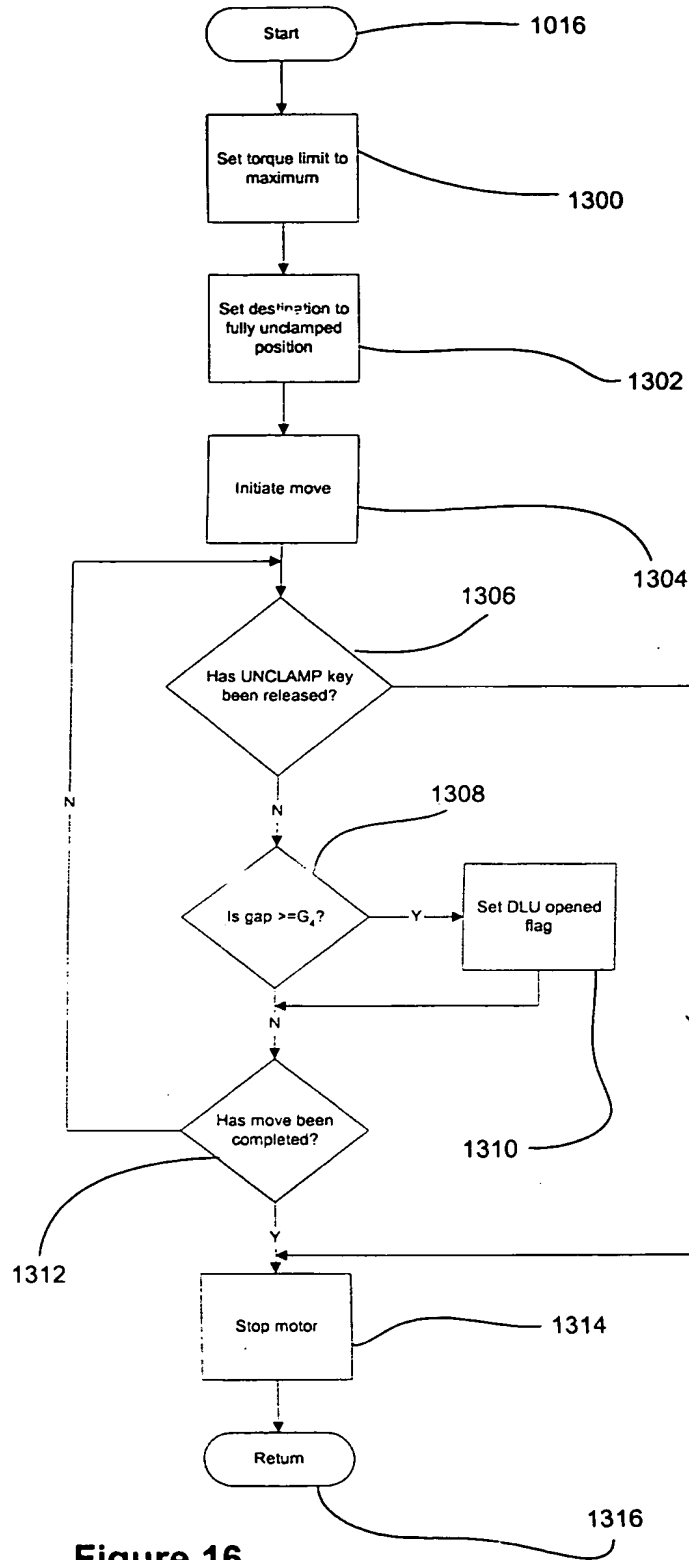


Figure 16

09236781.051804

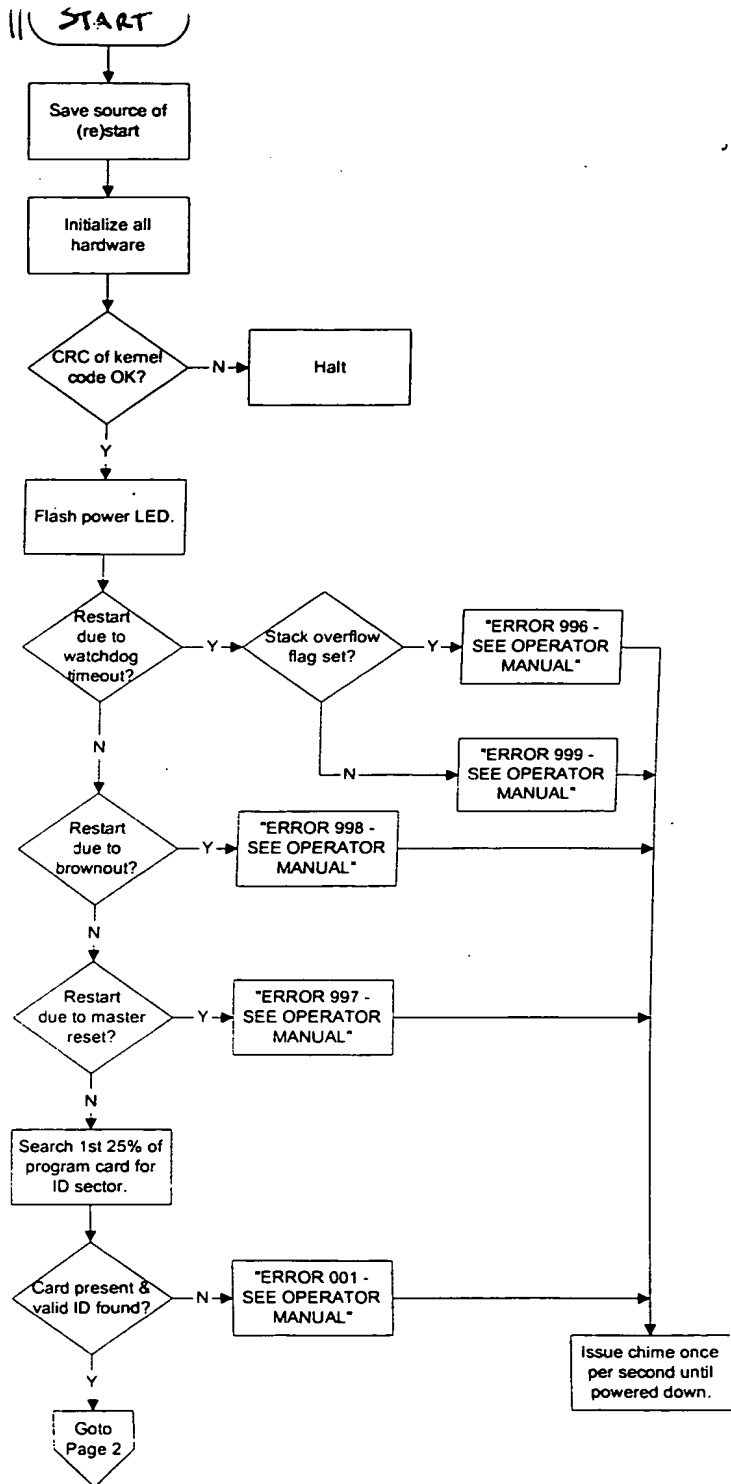


FIG. 17a

09036781.061801

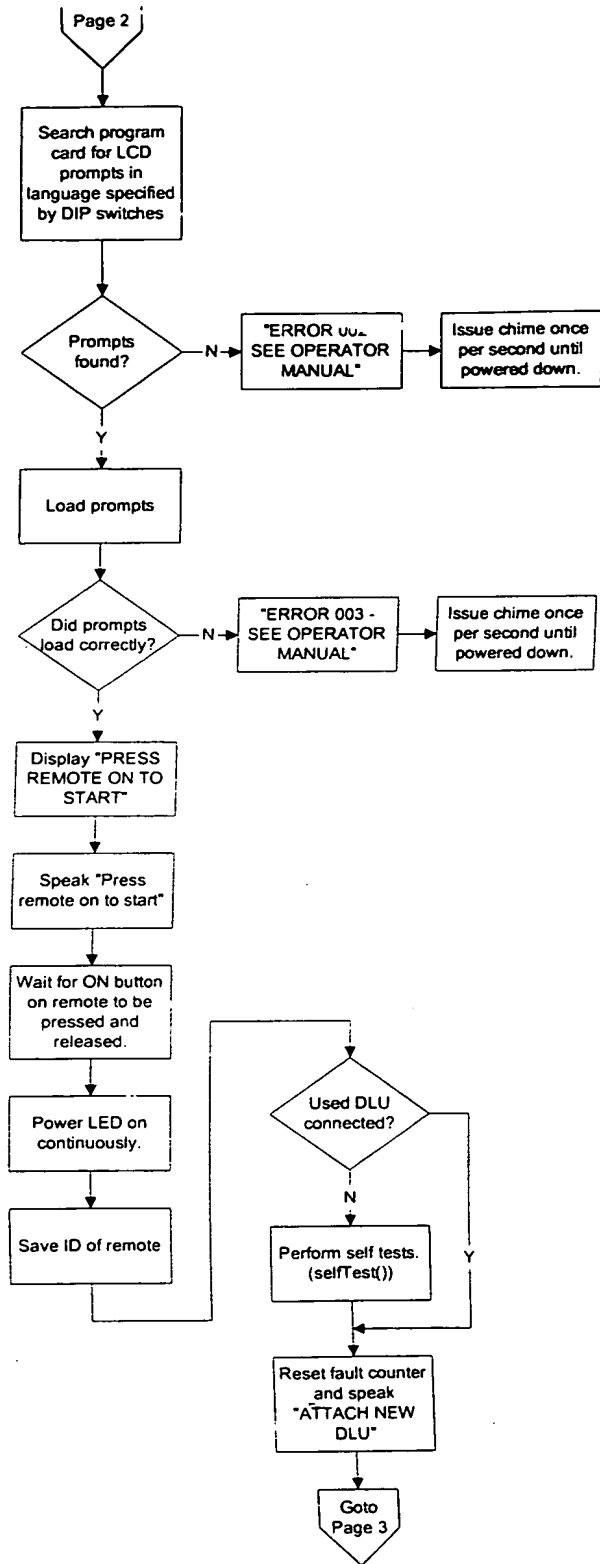


FIG. 17b



09836784 061804

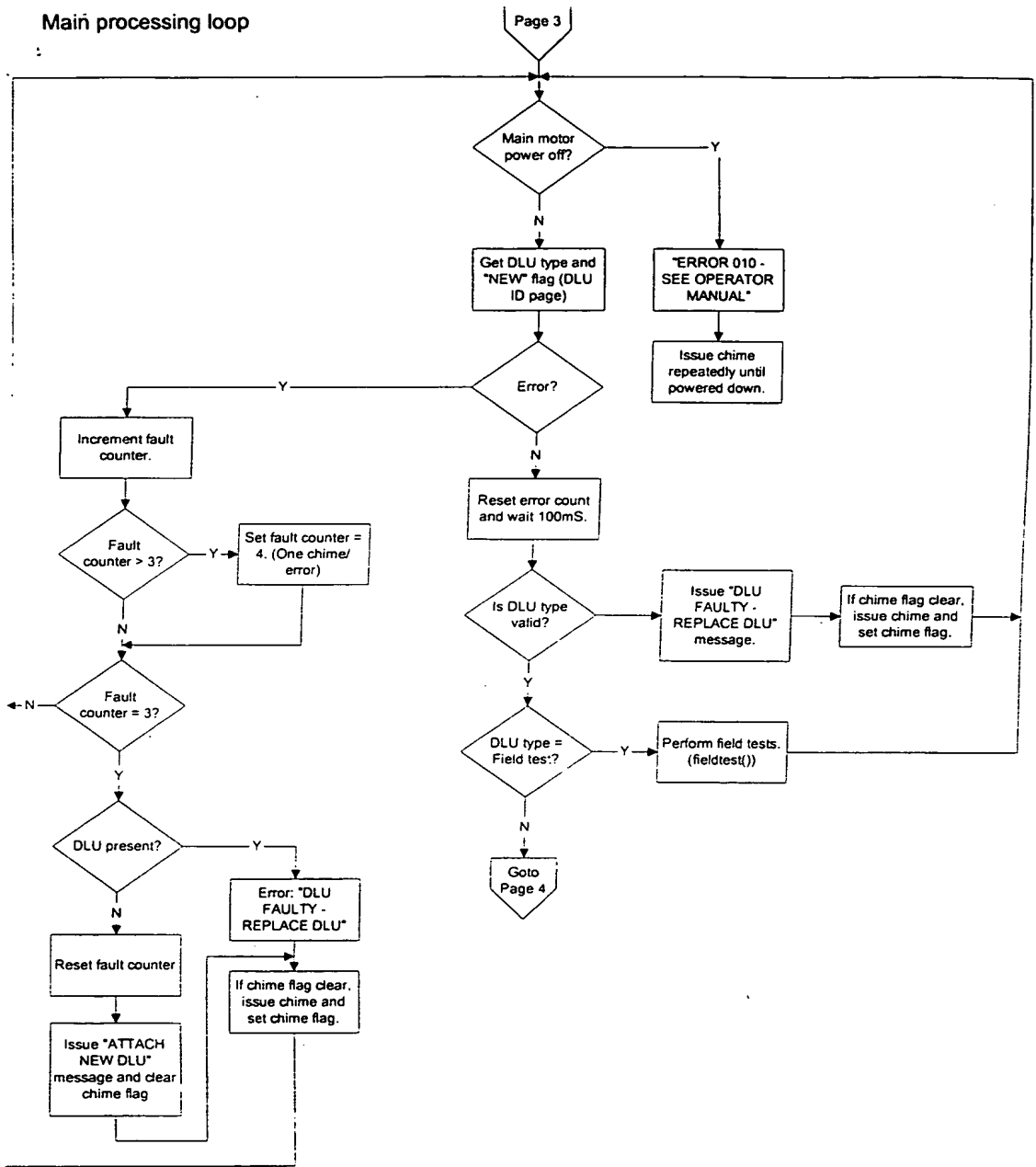


FIG. 17c

09836781 061804

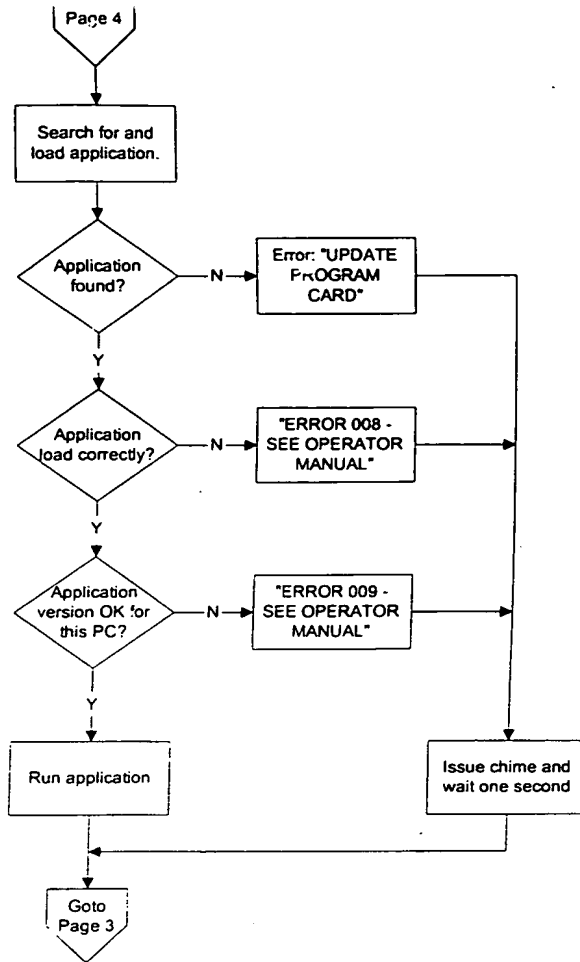


FIG. 17d

09036701 064304

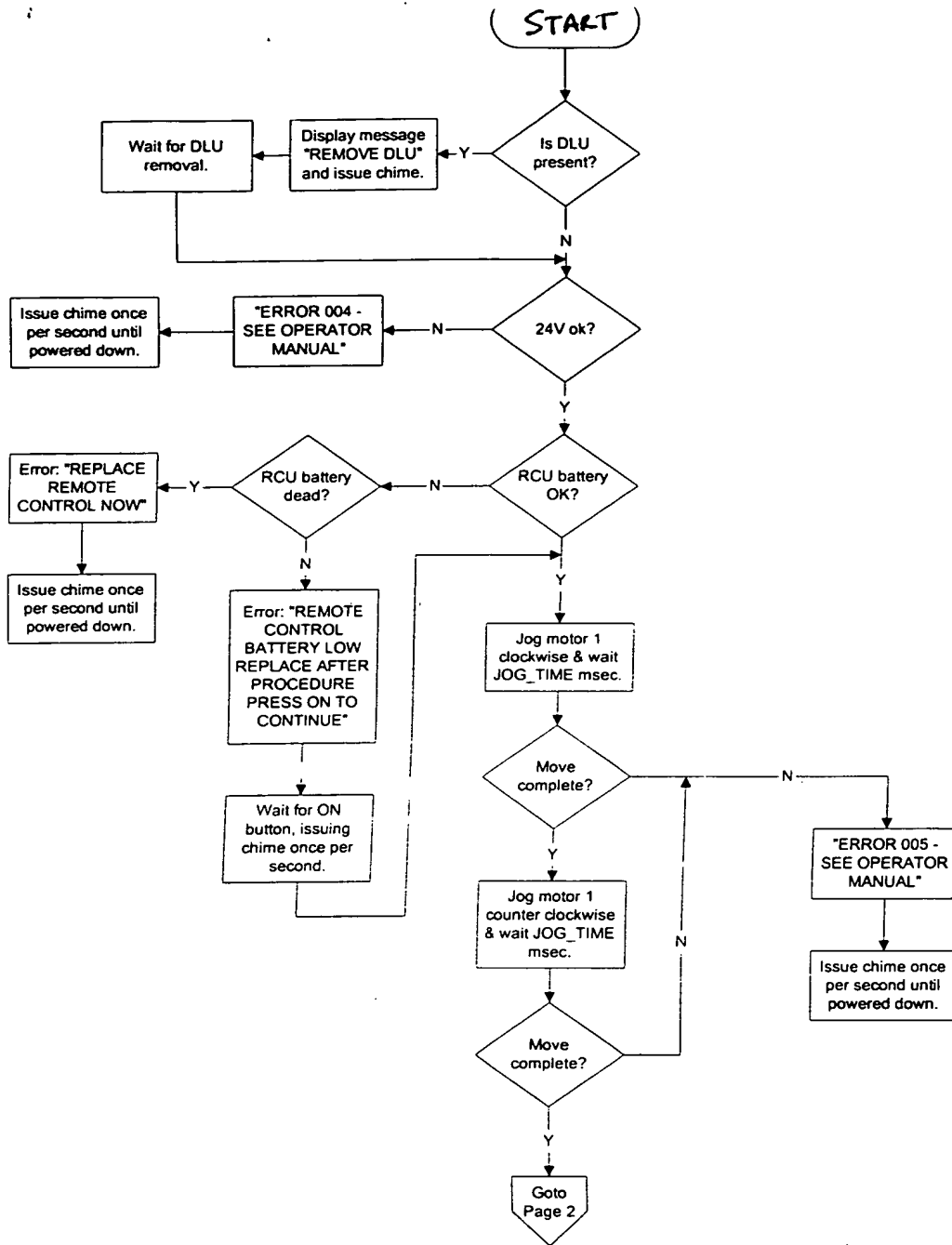


FIG. 18a

09036701 061001

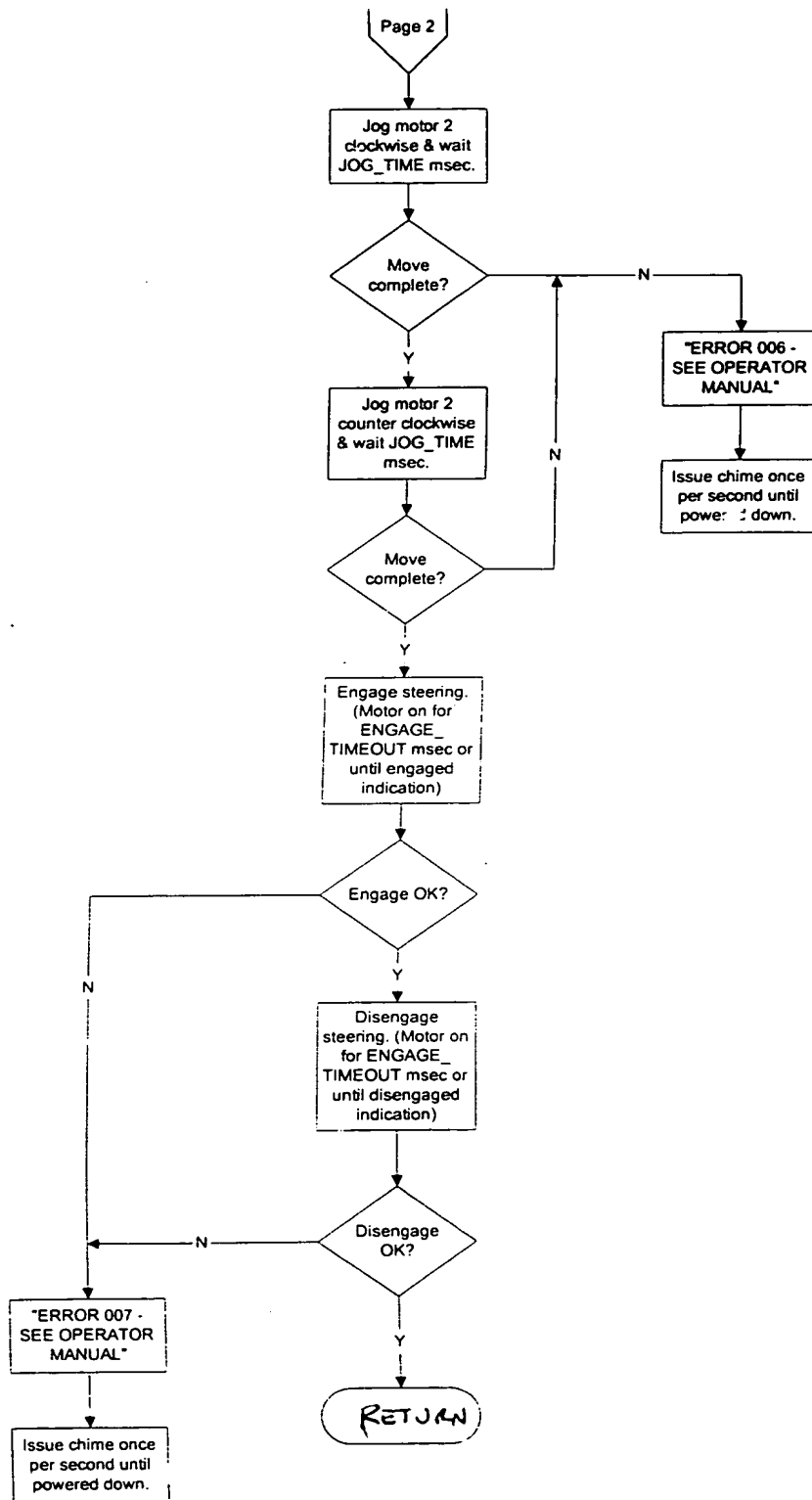


FIG. 186

09836784.064804

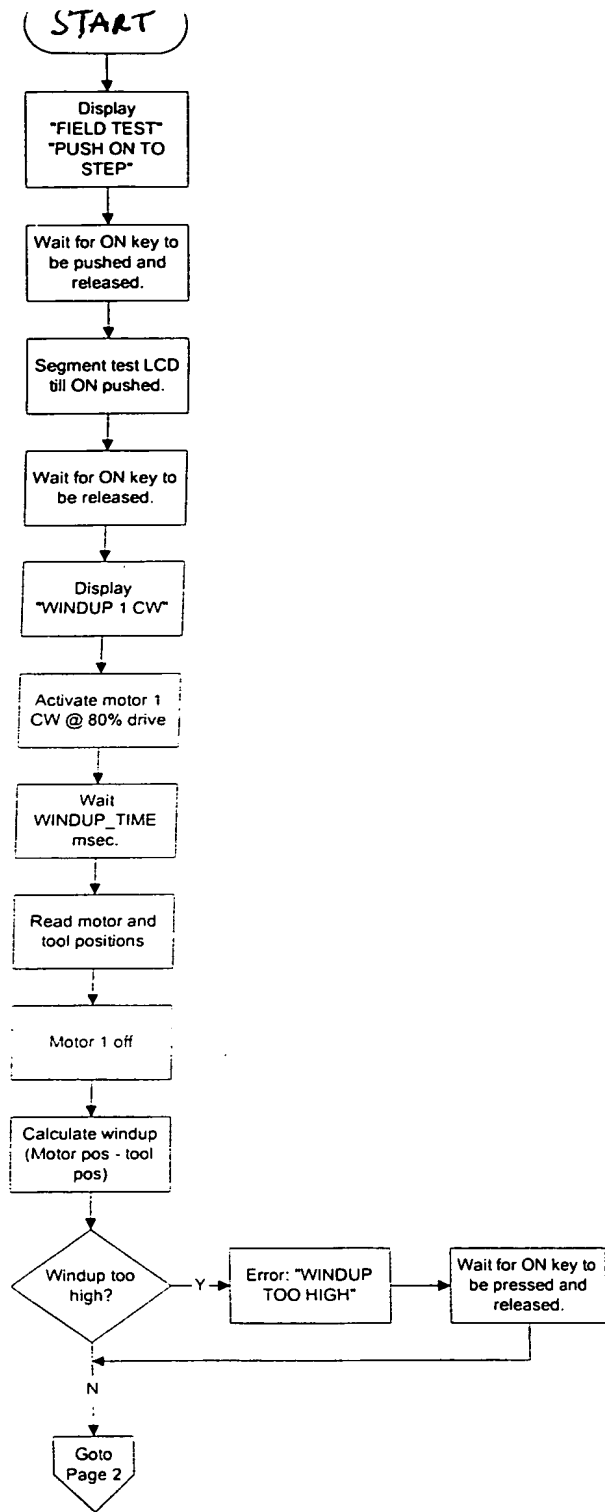


FIG. 19a

09036781.061804

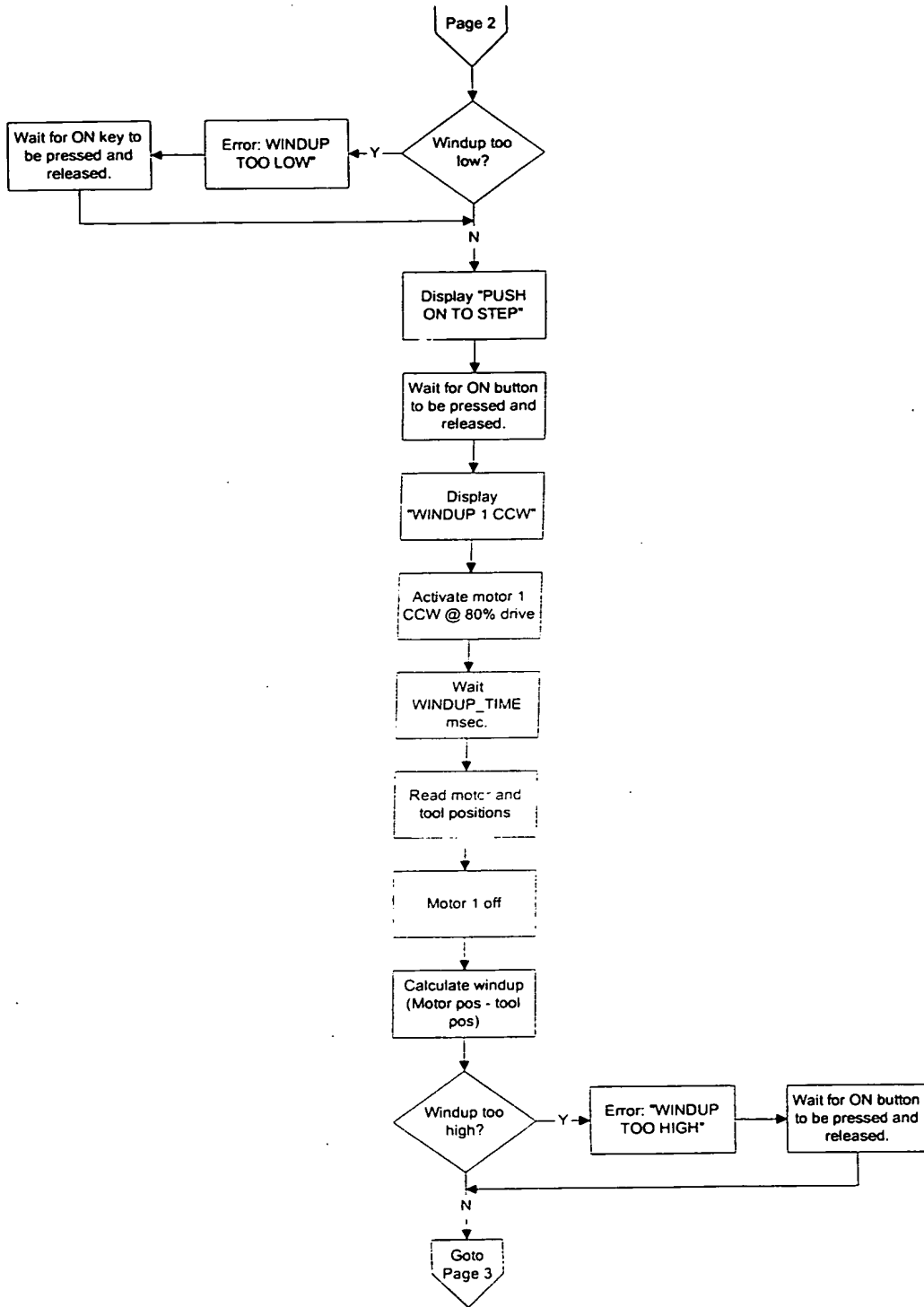


FIG. 196

09836781.061801

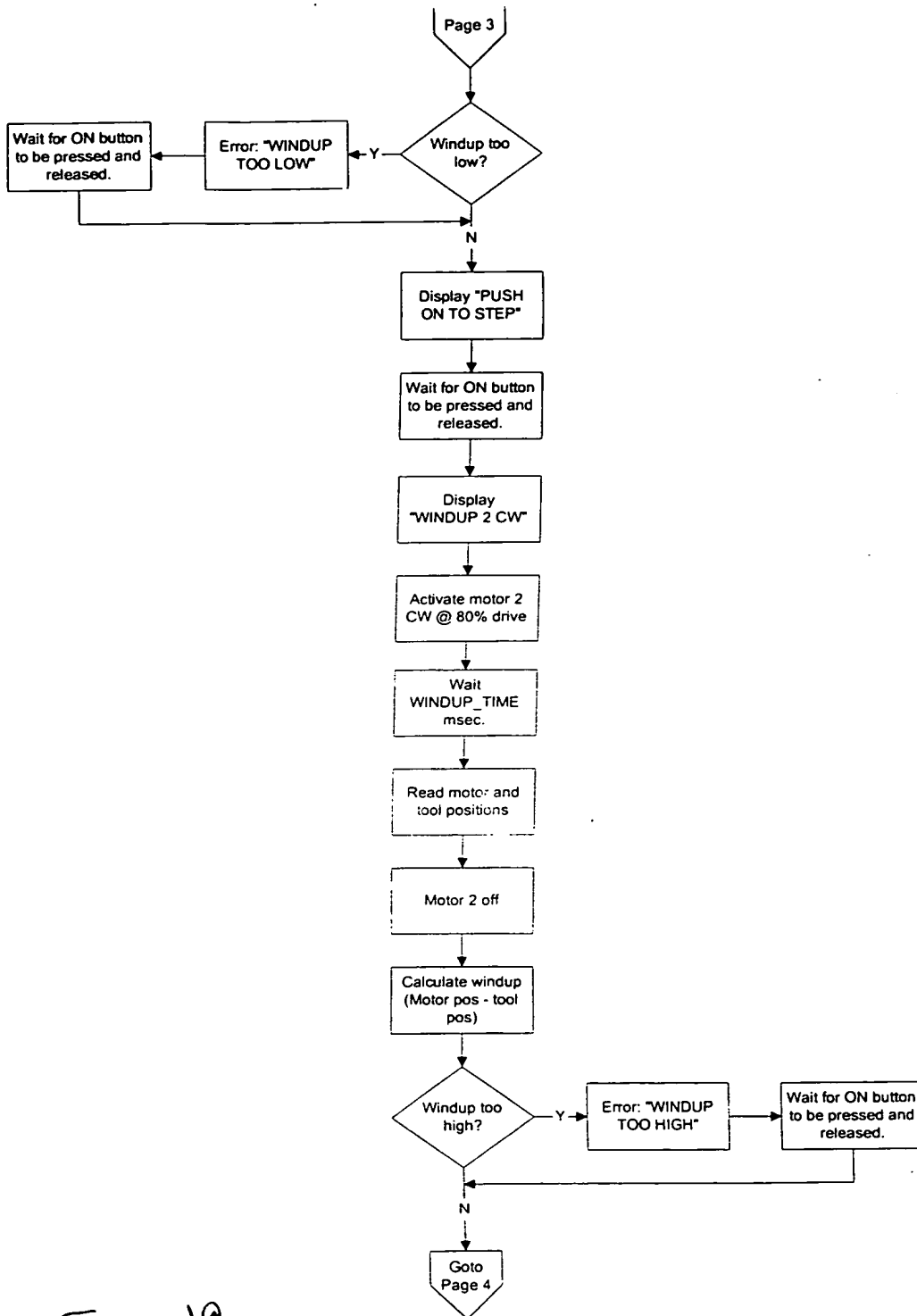


FIG. 19c

05836781-061801

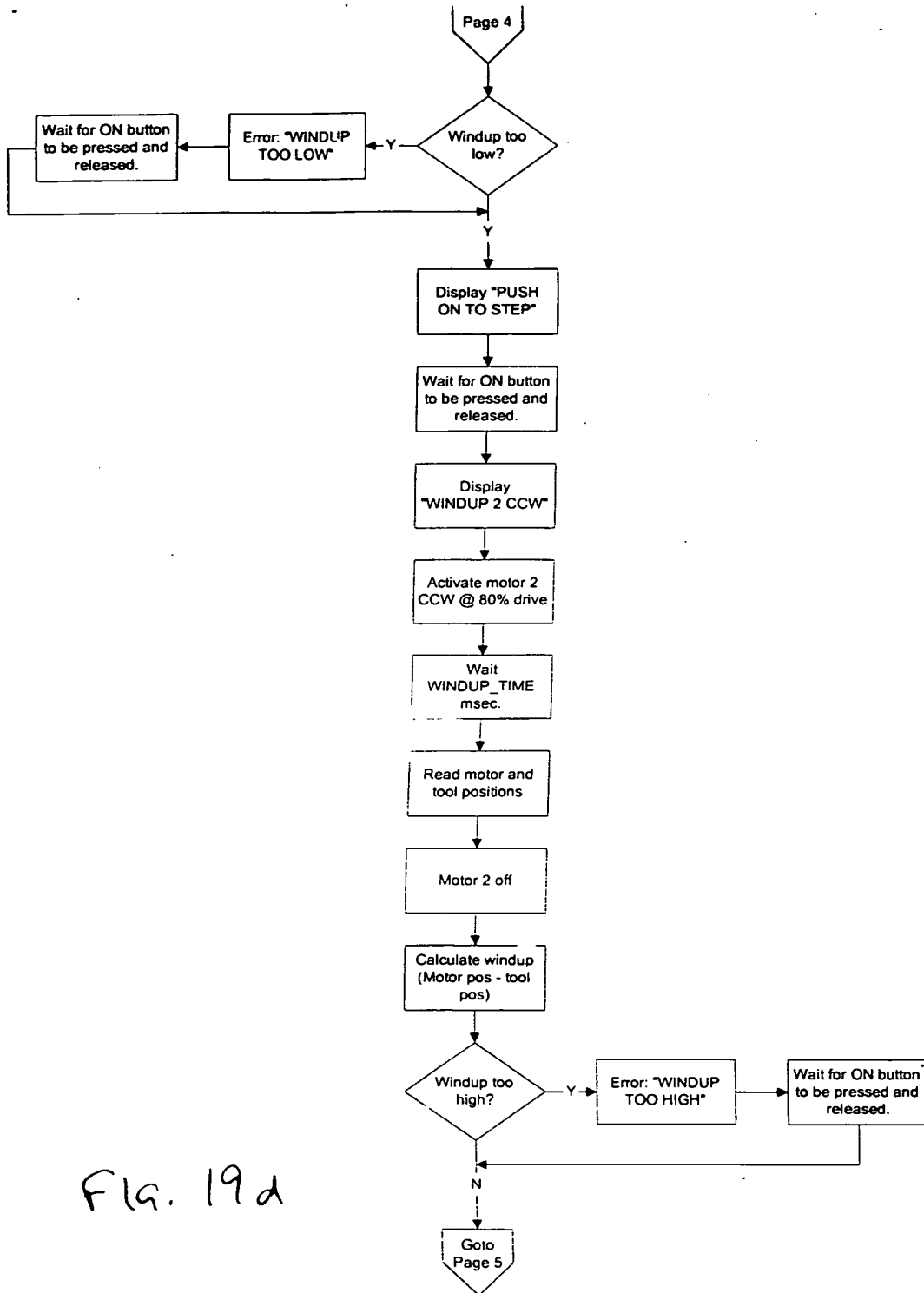


Fig. 19d





09836784 064804

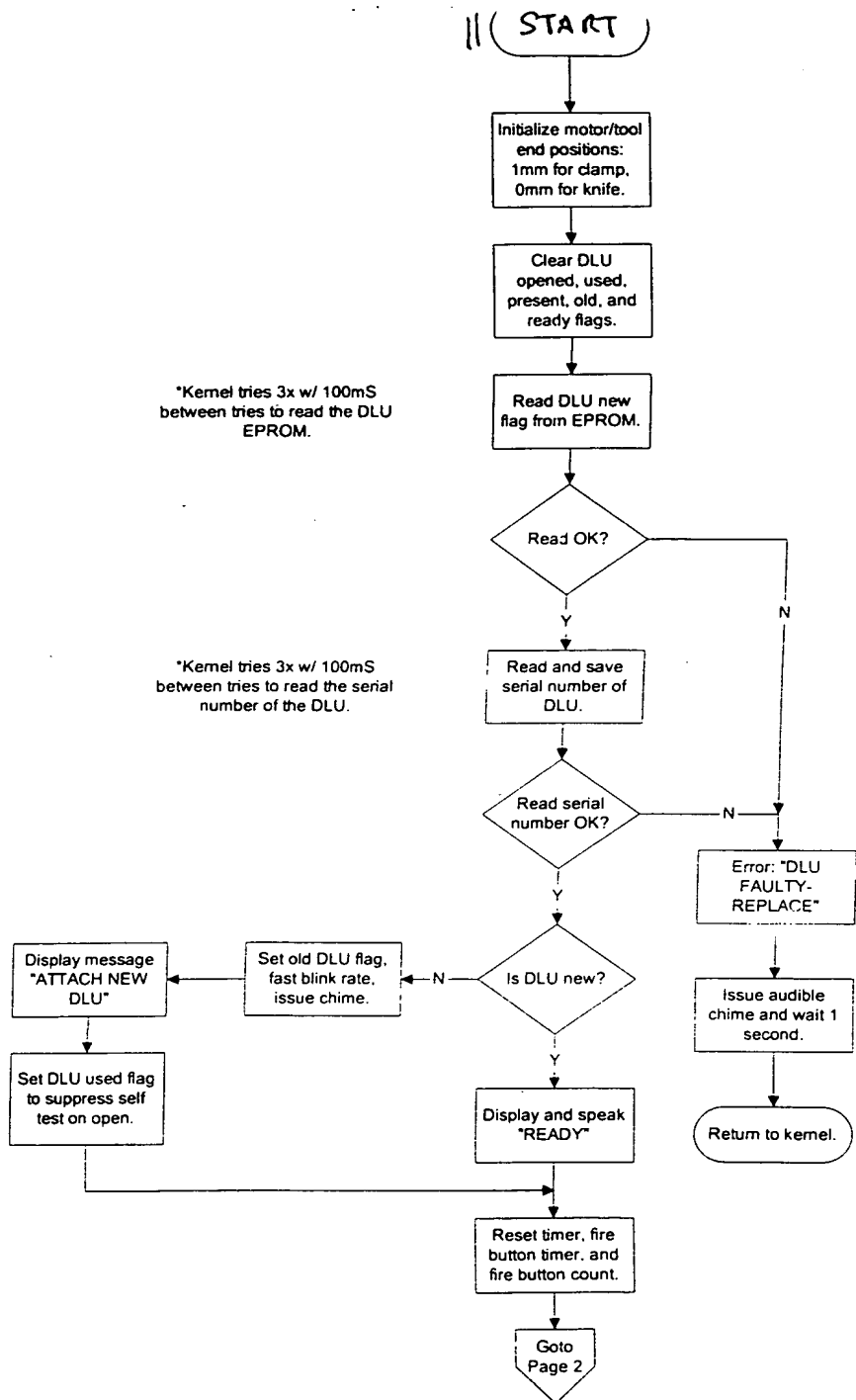


FIG. 20a

09836784.061804

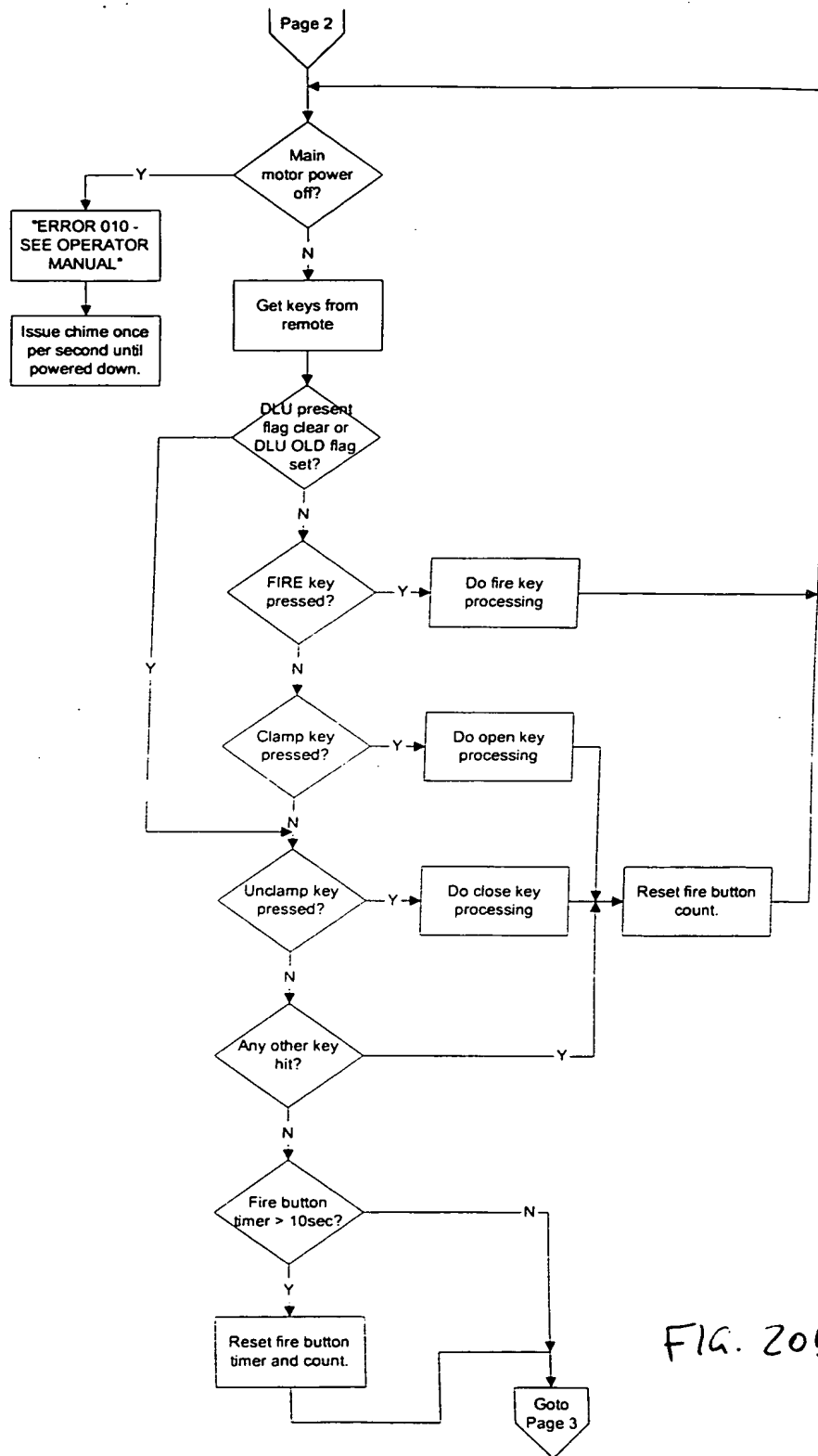
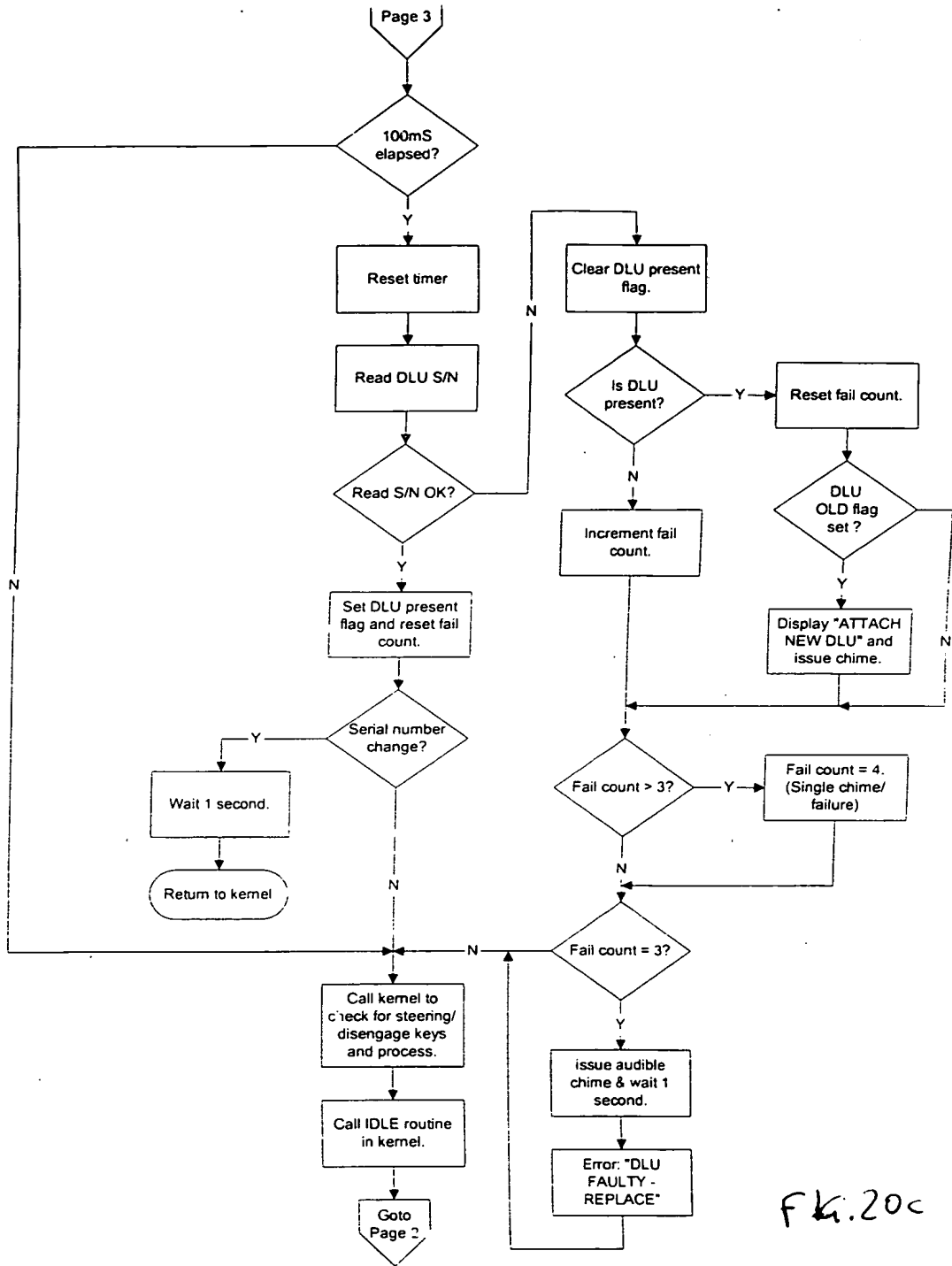


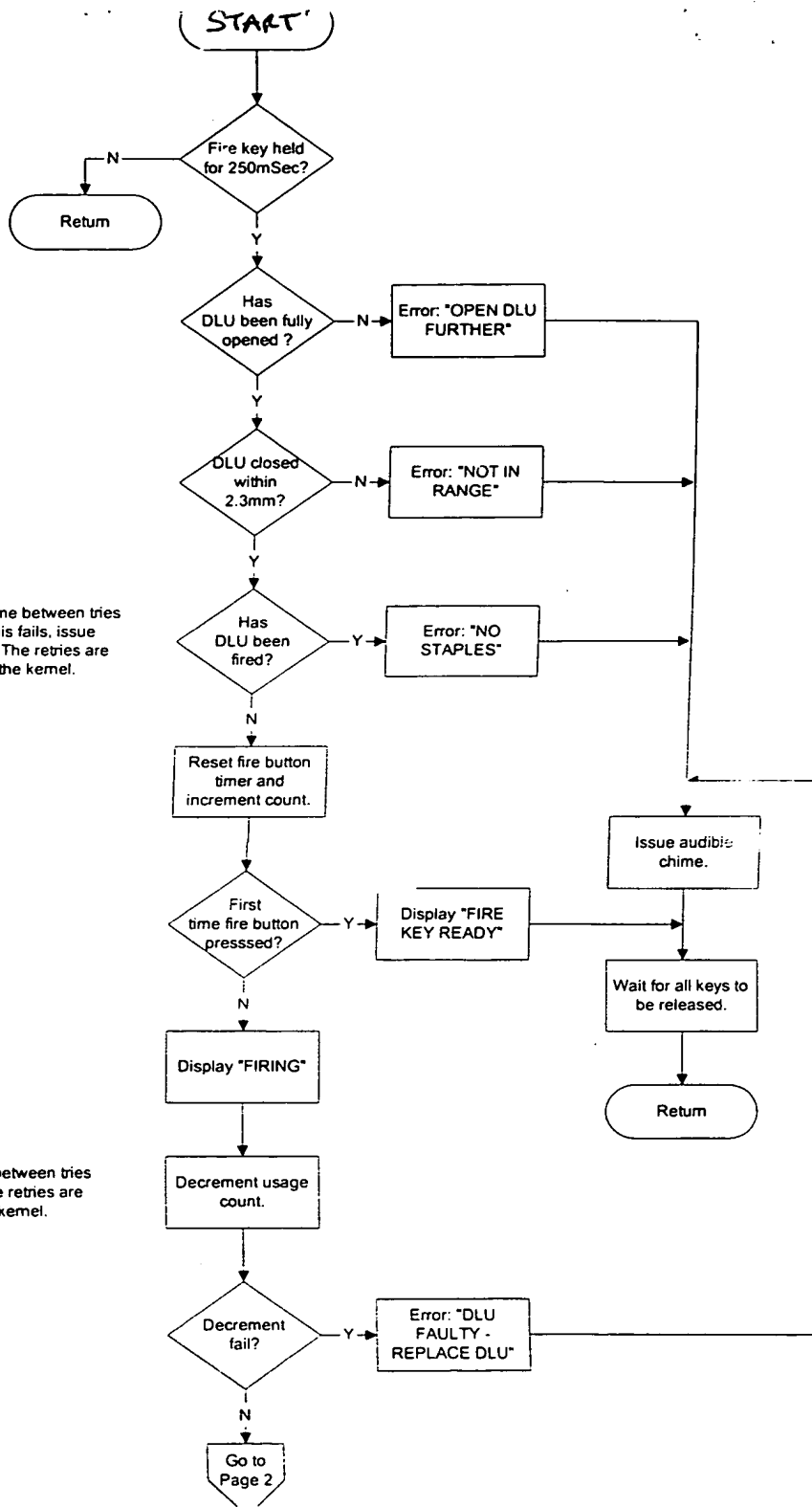
FIG. 205

090306787.067804



FK.20c

09836781 061801



\*Try 3x w/ 100mS time between tries to read DLU. If this fails, issue message and exit. The retries are performed by the kernel.

\*Try 3x w/ 100mS time between tries to decrement DLU. The retries are performed by the kernel.

FIG. 219

09836784 061804

Windup threshold is defined as SHAFT\_WINDUP\_MAX

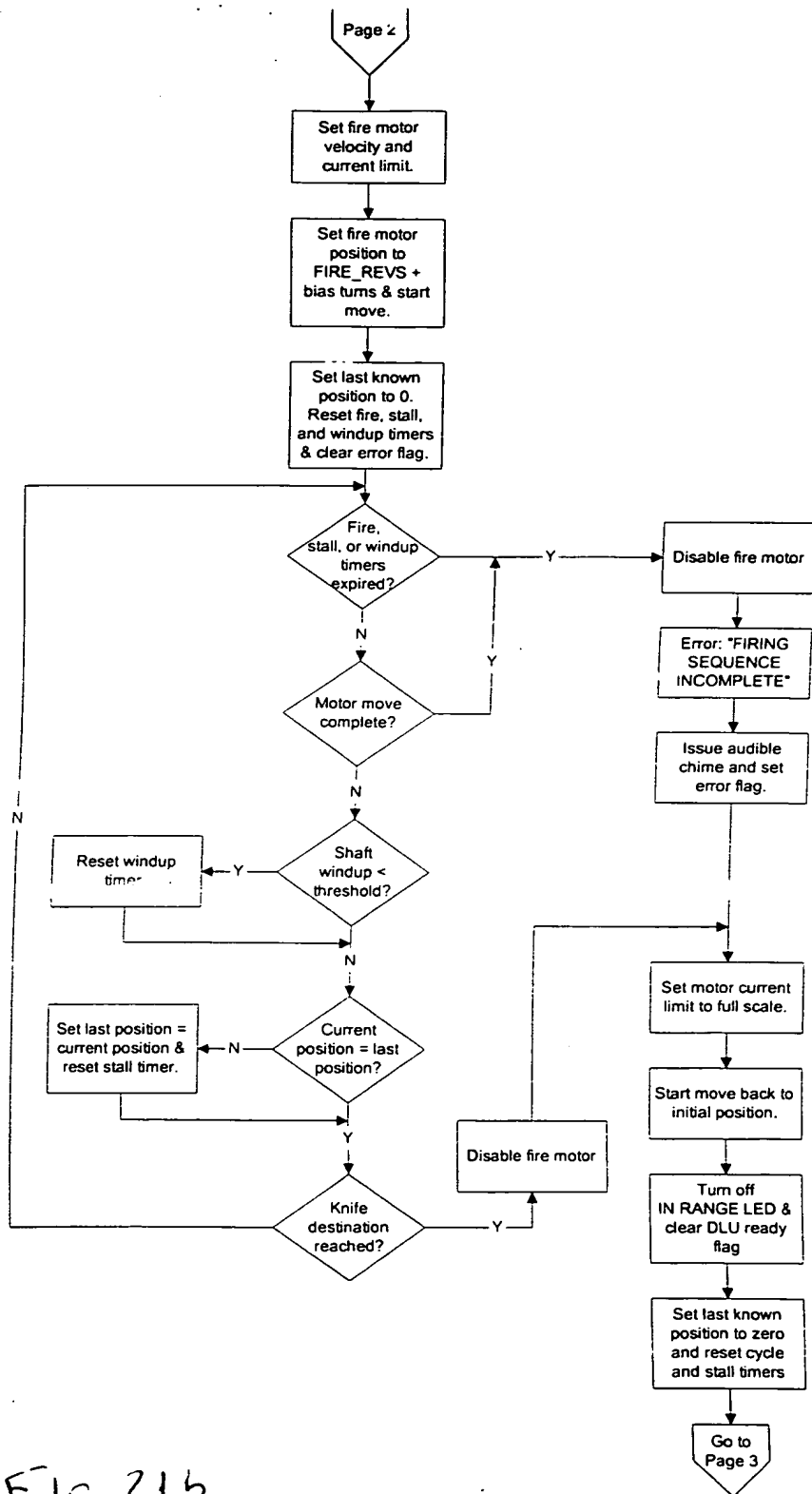


FIG. 21b

09836784.061801

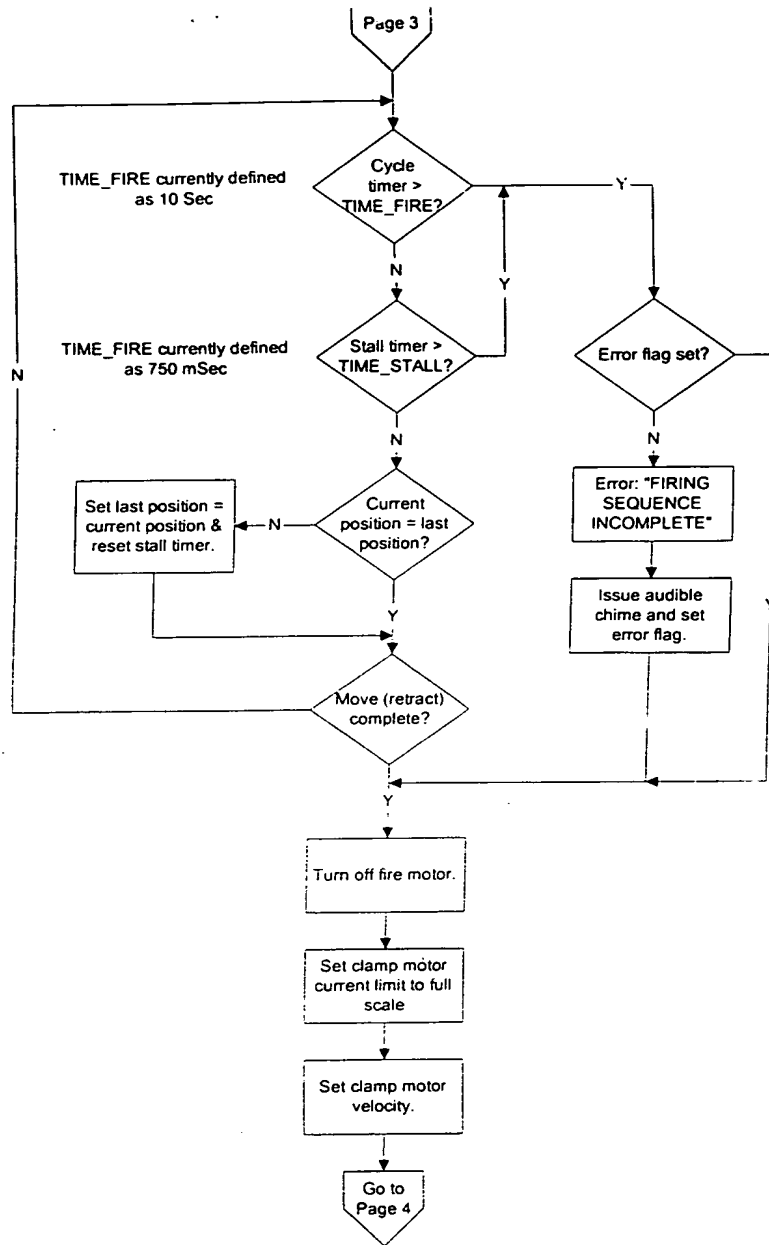


FIG. 21c

09836781 061801

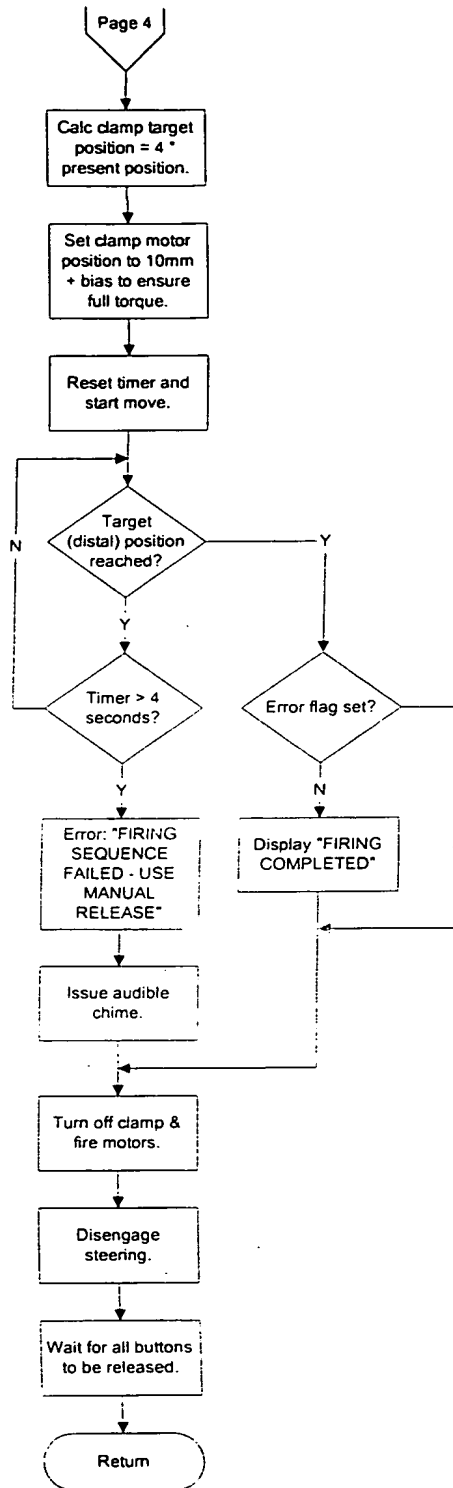


FIG. 21d



09836781.061801

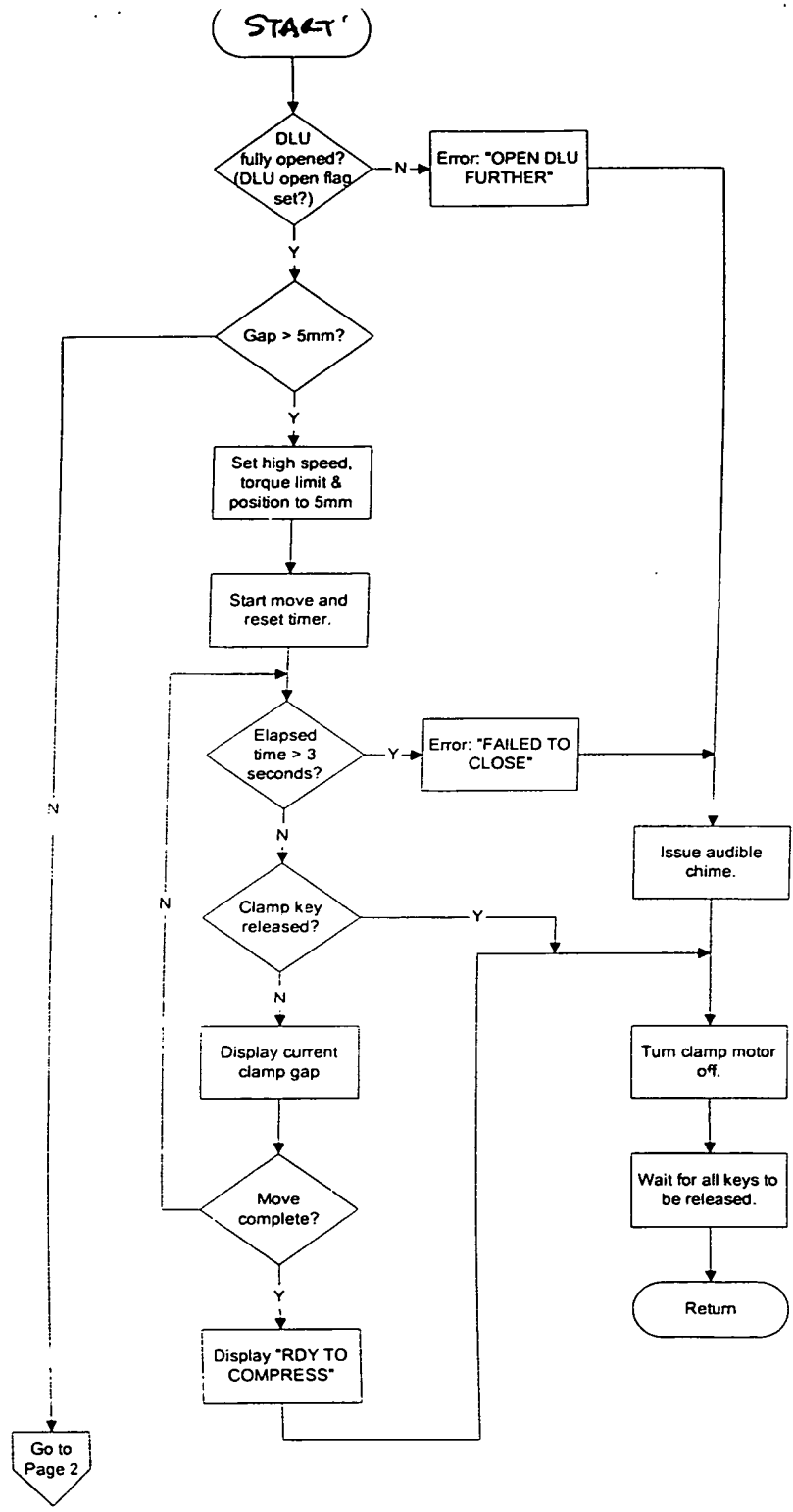


FIG. 22a

09036701 061801

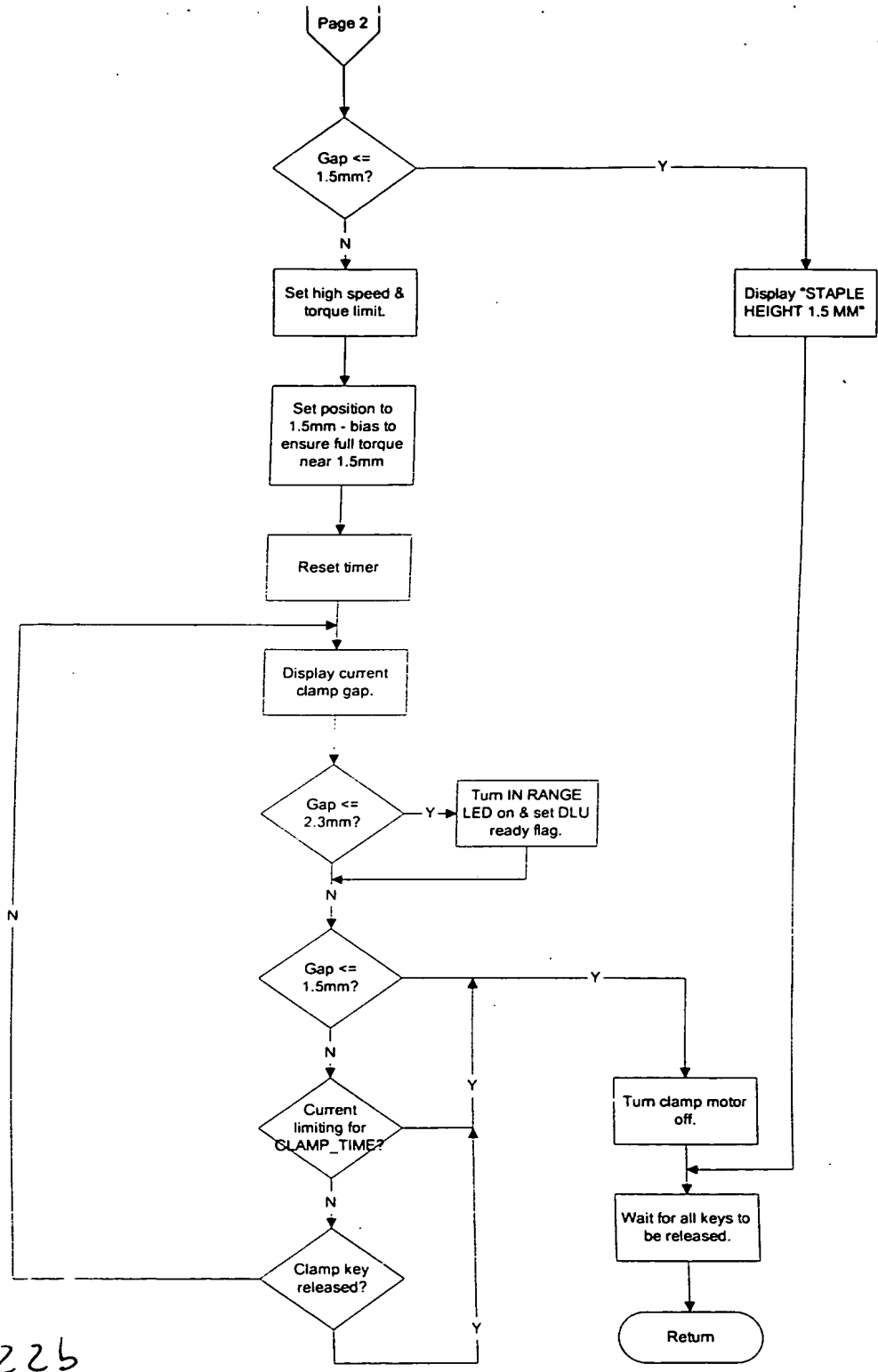


FIG. 22b

09036781.064801

\*The kernel tries 3x w/ 100mS time between tries to write DLU.

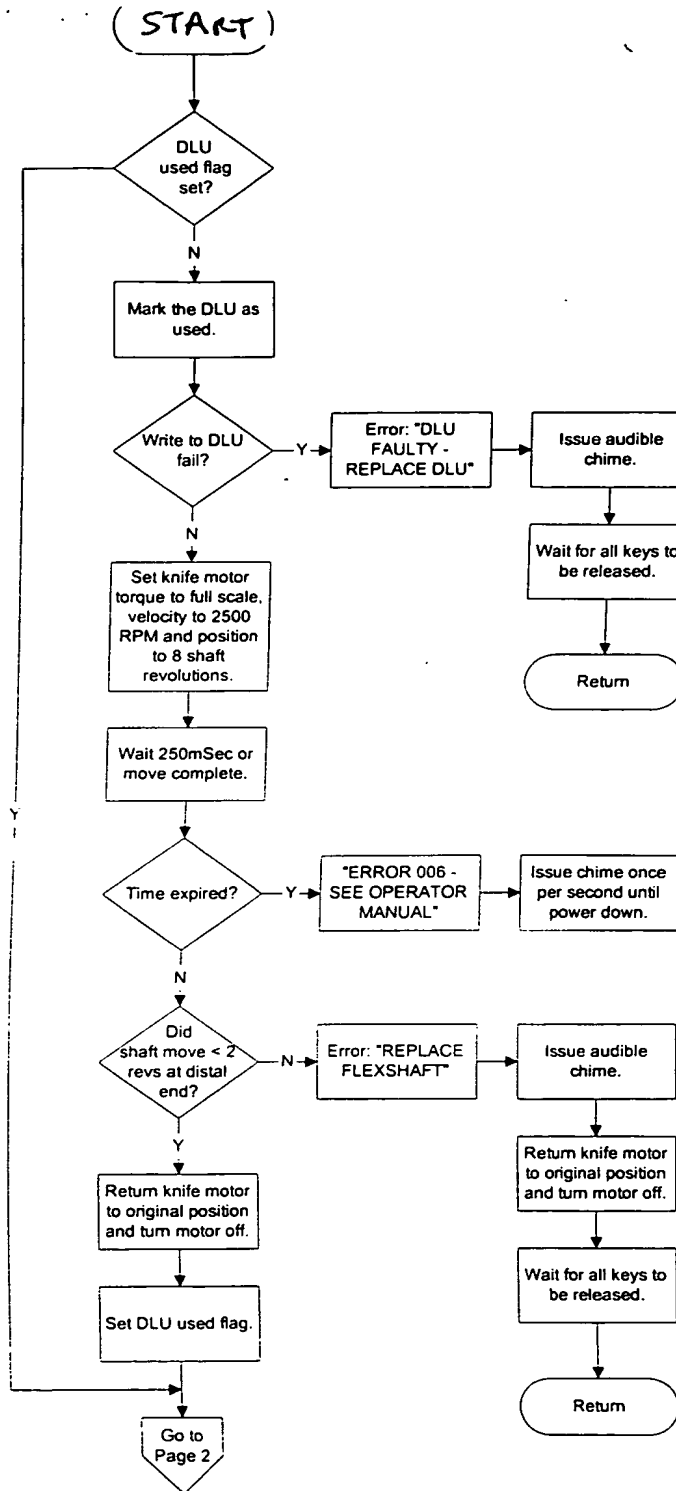


FIG. 23a

09836781.061801

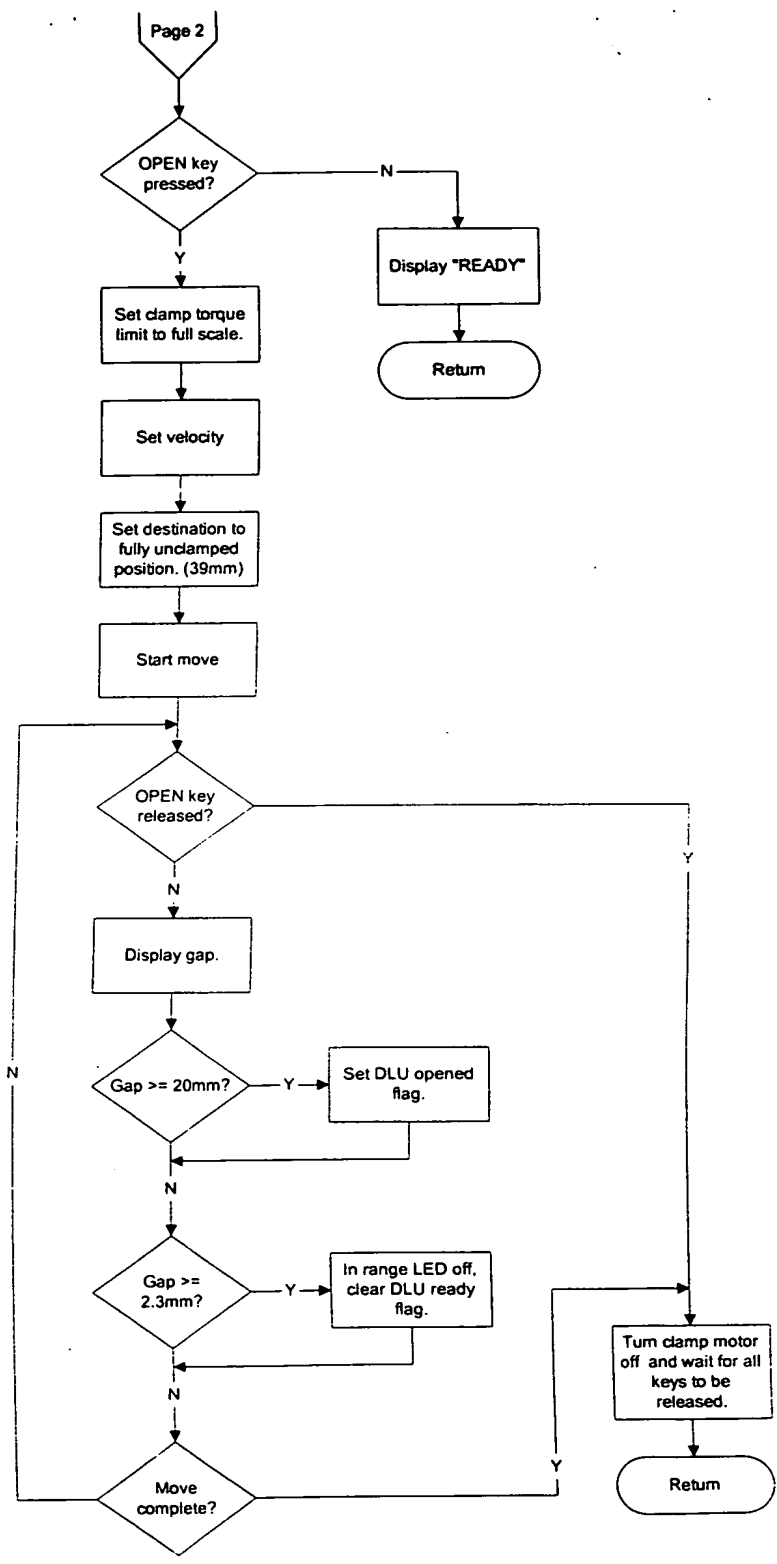


FIG. 23b